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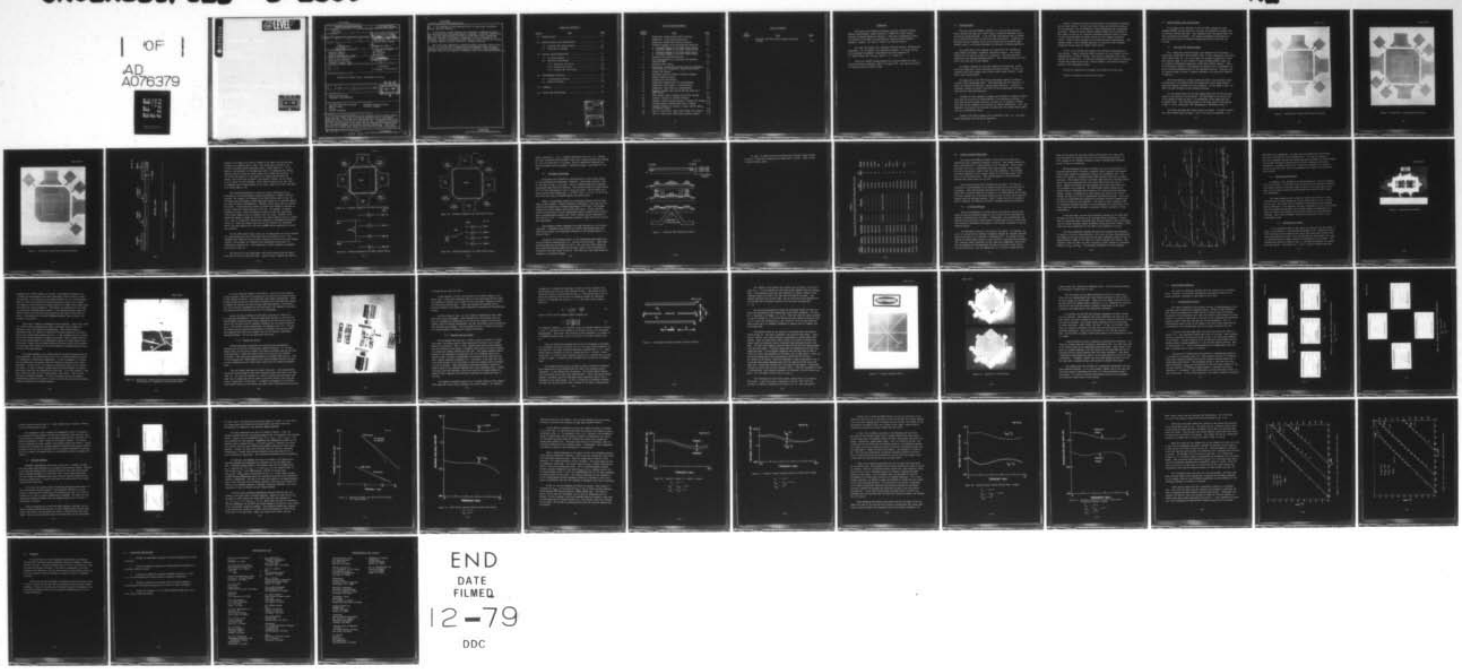

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The GaAs dual-gate MESFET is a very powerful microwave device offering more gain and a wider range of functional capabilities than a conventional single-gate FET. It has also been demonstrated that the dual-gate FET can be switched from full off to full on in less than 50 psec. Combining the high gain and fast switching speed of this device with its inherently high isolation makes it an attractive candidate for microwave switching applications. This report describes the progress made during the first year of an effort to demonstrate

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20. ... the feasibility of using dual-gate FET's as high speed, broadband, lossless microwave switches.

In this period, we have designed and fabricated two different dual-gate FET structures which functionally operate as multipole, multithrow switches with gain. We have achieved gains of 18 dB at 10 GHz from a more conventional dual-gate structure. This result is comparable to the best reported in the literature. We have also measured on-off ratios in excess of 30 dB and channel-to-channel isolation in excess of 25 dB in a multiport structure.

Due to the many difficulties in handling multiport structures such as these, we have not yet been able to demonstrate actual microwave signal switching. However, near the end of this report period we developed a new measurement technique which has the potential of eliminating many of the existing difficulties.

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FOREWORD

This report was prepared by Raytheon Company, Research Division, Waltham, Massachusetts, under Contract No. N00014-78-C-0623, entitled "Lossless Broadband Microwave Switches." This work is administered under the direction of the Office of Naval Research, Material Sciences Division, Arlington, Virginia. Mr. Max N. Yoder is the contract monitor.

The work was carried out at Raytheon Research Division, Semiconductor Department. Mr. R. Bierig is the department manager. Dr. James Vorhaus is the principal investigator. Experimental work was performed by Dr. Walter Fabian, Mr. Paul Ng, and Mr. J. E. Curtis, Sr.

This is the Interim Technical Report for Contract N00014-78-C-0623. It covers the period 1 September 1978 to 31 August 1979. The report was given the Raytheon internal number S-2609.

1.0 INTRODUCTION

The GaAs dual-gate MESFET (DGFET) is a very powerful microwave device offering more gain and a wider range of functional capabilities than a conventional single-gate FET. It has also been demonstrated that the DGFET can be switched from full off to full on in less than 50 psec. Combining the high gain and fast switching speed of this device with its inherently high isolation makes it an attractive candidate for microwave switching applications.

The overall goal of this program is to demonstrate the feasibility of using DGFET's as lossless, broadband, microwave switches. The specific vehicles for this work are a pair of multichanneled, dual-gate structures originated at the Raytheon Research Division. This report describes the work done in the first year of this program.

At program inception we had paper designs for double-pole, double-throw and single-pole, 4-throw dual-gate FET switch devices. We have now fabricated from those designs actual devices which exhibit multipole, multi-throw switch characteristics.

We began with a basic FET process technology capable of producing standard X-band single-gate FET's. That technology has been improved, refined, and adapted for dual-gate multichanneled structures. Among the significant changes are etched "via-holes" for source grounding and integral beam leads for chip interconnection.

Possibly our most significant progress and certainly our biggest problems have come in the area of rf characterization of the dual-gate structures. A great deal has been learned about how, and how not, to measure a DGFET; what kind of bias conditions are necessary for optimum performance; and, most important, what kind of test fixturing is needed when the device being studied has up to 9 independent ports.

Details of the device designs will be described in Sec. 2.0. The fabrication technology used will also be presented.

Section 3.0 presents various characterization and measurement techniques used on these devices. We have been able to adapt and extend conventional dc, low-frequency, and rf techniques to these significantly more complicated structures. Among the unique methods employed which will be presented in this section are the use of a computer-controlled automated system to handle I-V type characterization of devices and the use of a coplanar microstrip alumina circuit to allow simplified and accurate microwave measurements. This coplanar circuit is also a possible precursor to eventual on-chip monolithic integrated circuits using the DGFET switch devices.

In Sec. 4.0 we present the results of our microwave measurements on these devices. Using a simplified DGFET structure as a test vehicle, we have achieved gains of 18 dB at 10 GHz. This result is comparable to the best reported in the literature. To determine feasibility of these devices as switches, we have also studied on-off ratios, reverse isolation, and channel-to-channel isolation, with encouraging results.

Section 5.0 summarizes our progress and results in the past year.

Section 6.0 outlines our plans for the future.

2.0 DEVICE DESIGN AND FABRICATION

At the outset of the contract we had two similar designs for multi-channeled DGFET devices which had, on paper, the potential for being useful as microwave switches with gain. Our experience with conventional FET's and GaAs processing was extensive. The process technology in particular was quite mature and gave an excellent starting point for the work that was to follow.

2.1 Dual-Gate FET Switch Designs

Two multichannel switch structures were designed for this program, a double-pole, double-throw device (DPDT) (Fig. 1) and a single-pole, four-throw device (SP4T) (Fig. 2). As a test vehicle, we designed a third kind of dual-gate structure (Fig. 3) that consists of a pair of simple DGFET's which can be considered independent single-pole, single-throw (SPST) switches. These three structures clearly do not constitute an exhaustive set of possibiliities for switch transistor geometries based on the dual-gate structure. However, they are general enough to permit a realistic evaluation of the potential of DGFET's as switches.

Each chip consists of a large central pad which is the transistor source. Arrayed about it are external pads that provide the various drain contacts. Each drain defines a channel of 150 μm periphery. As can easily be seen, the DPDT and SP4T devices are four-channel structures.

In each channel there are two gate fingers which are end fed from pads located at the corners of the structure. The gate finger on the source side of the channel is known as gate 1, or alternatively as the signal gate (its functional name). The other gate finger (on the drain side of each channel) is gate 2, or the control gate. This arrangement is illustrated in Fig. 4.

The simple dual-gate FET switch operates as follows. The FET is biased for normal maximum gain operation; that is, the source is grounded, a dc

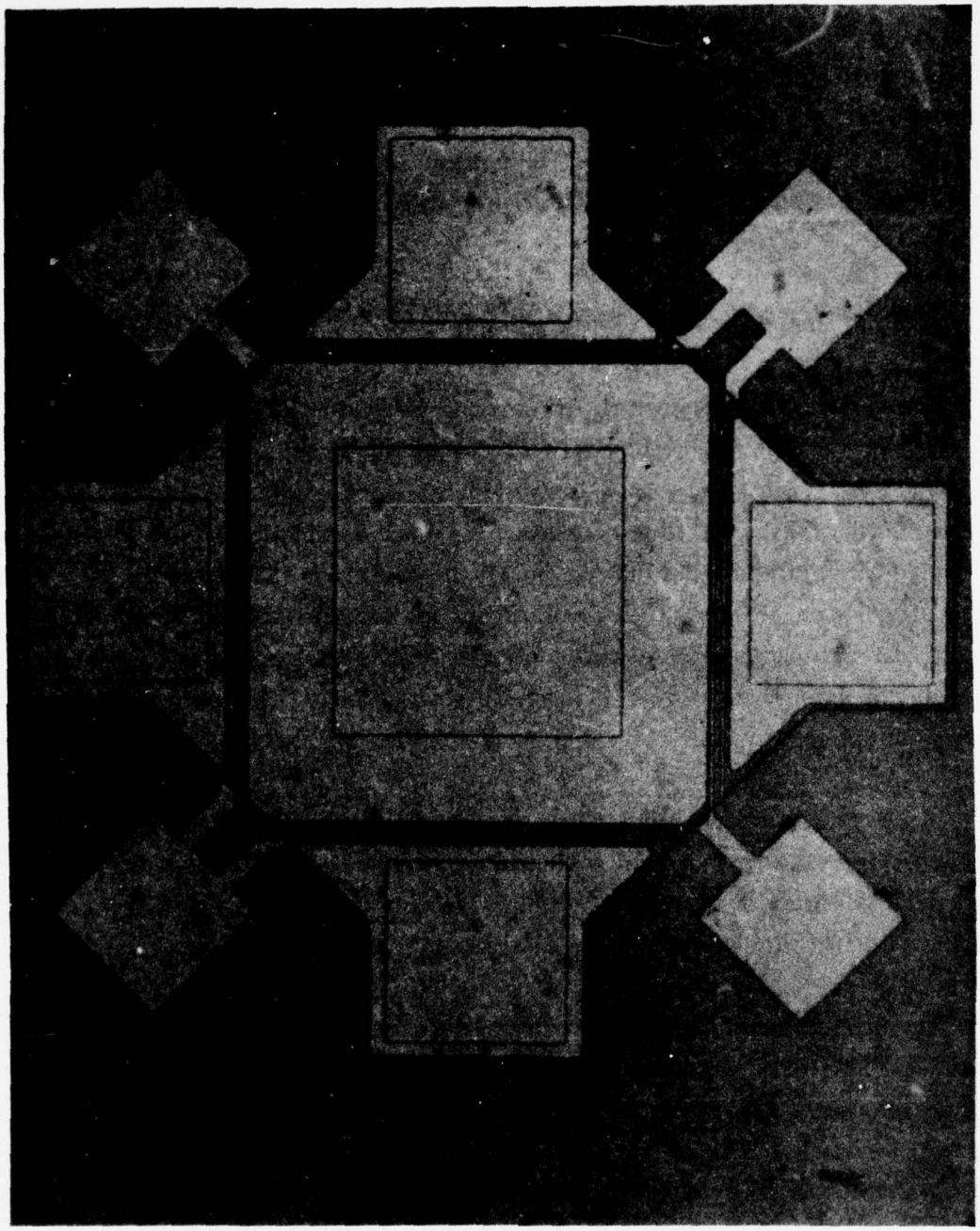

Figure 1. Double-Pole, Double-Throw Switch Structure.

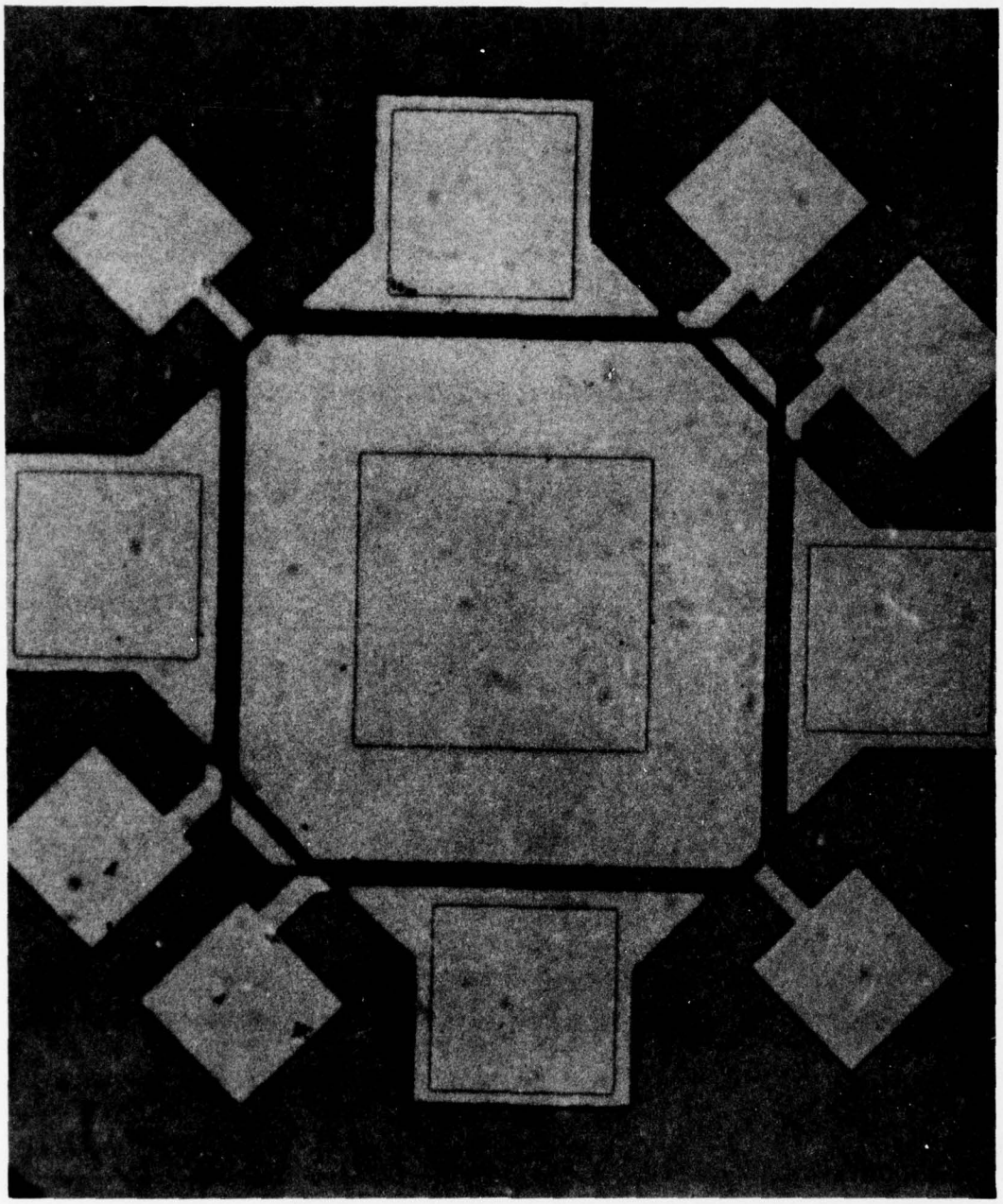

Figure 2. Single-Pole, 4-Throw Switch Structure.

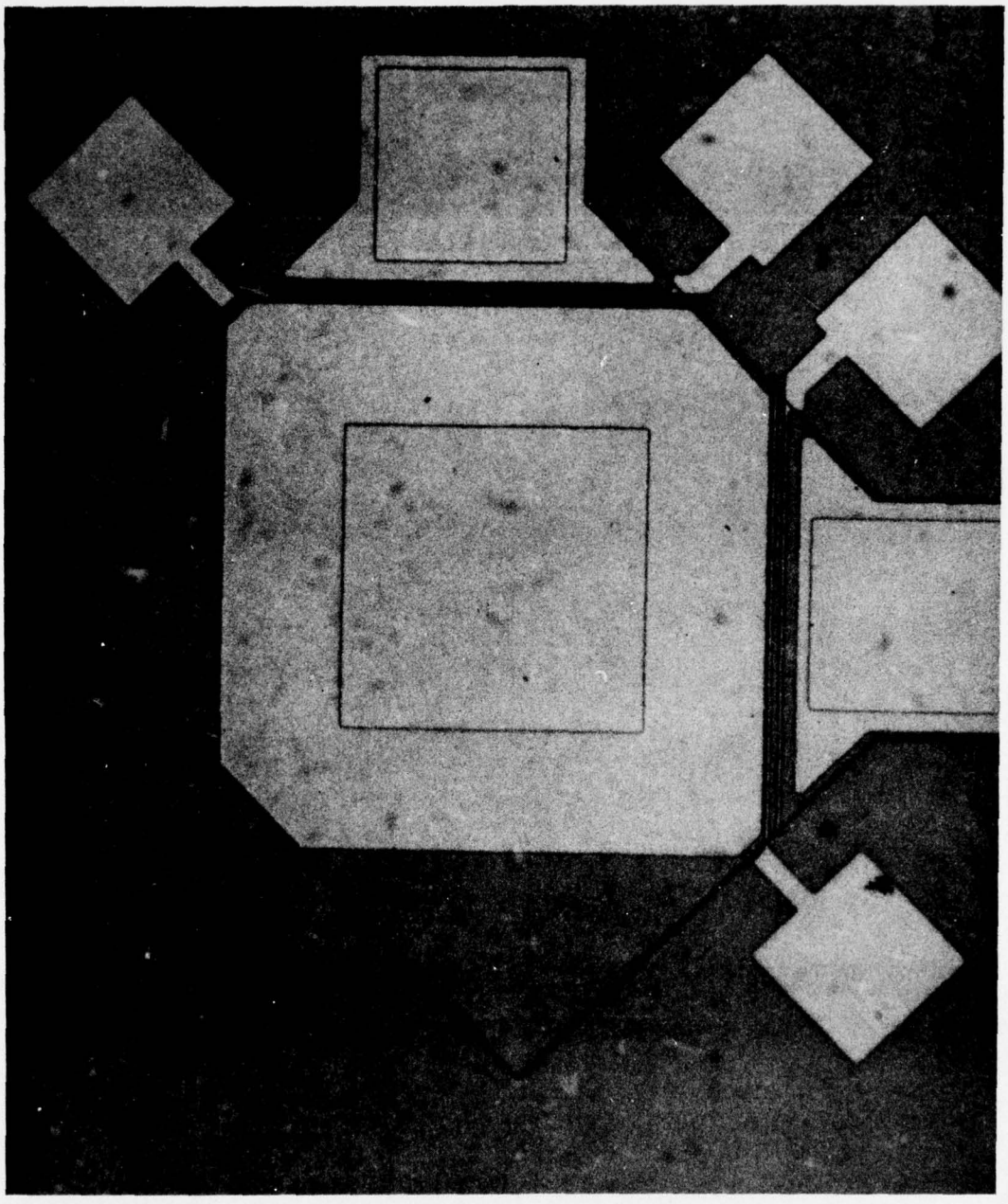

Figure 3. Single-Pole, Single-Throw Switch Structure.

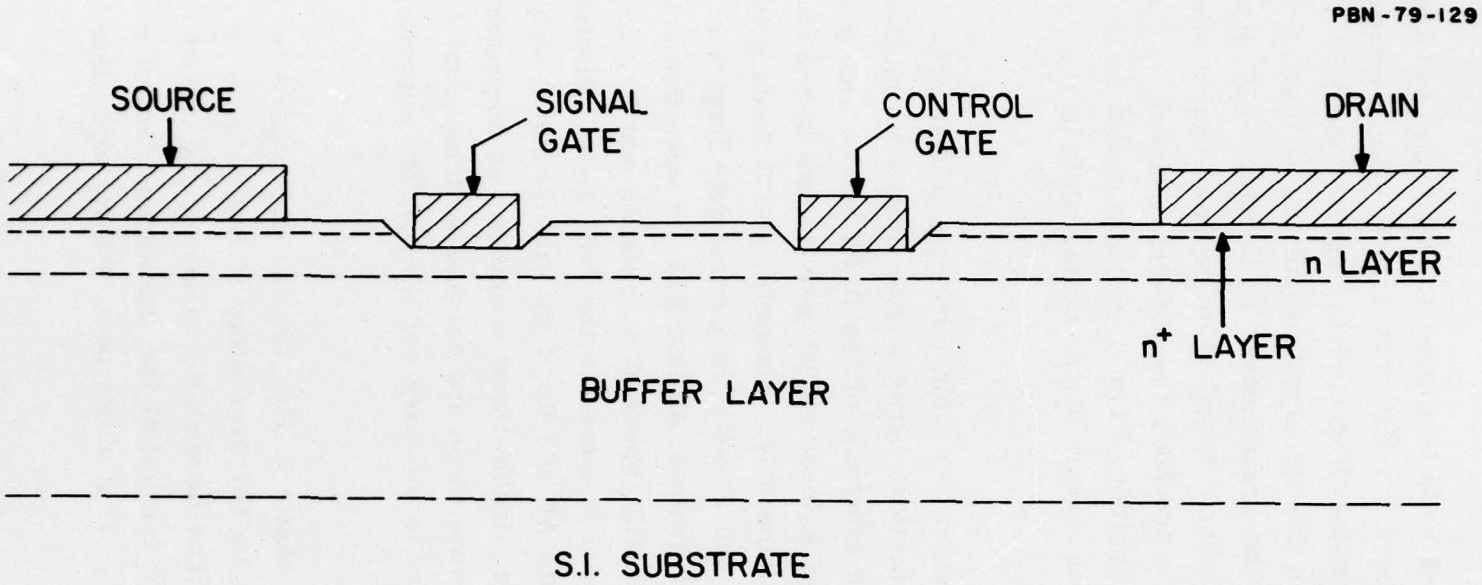

Figure 4. Schematic Diagram of the Dual-Gate FET Structure.

voltage in the range of 3-5 volts is applied to the drain, and the first gate is biased at or slightly above 0 volts. The second gate is biased as far forward as possible without injecting current, usually about +2 V. An rf signal is now impressed on the signal gate (gate 1), modulating the channel depletion depth and thus the drain current as in normal FET operation. If the control gate (gate 2) is now biased at or beyond channel pinch-off voltage, the current flow is blocked, the channel is closed, and the switch is in an "open" or "off" condition. Thus, with the device in its "on" state, an amplified input rf signal appears at the drain, while in the "off" state there is no output signal at all.

The functional definition of a multi-port chip is determined by the patterning of the interconnections between gate fingers in adjacent channels. Consider, for example, the schematic of the DPDT device shown in Fig. 5a. The signal gate pad labeled A feeds signal gate fingers in the channels defined by drains Aa and Ab simultaneously. Similarly, pad B feeds gates in channels Ba and Bb. Control gate pad a feeds the control gate fingers in channels Aa and Ba, while pad b feeds channels Ab and Bb. In operation, rf signals impressed at pads A and B will appear at outputs Aa and Ba, respectively, if the control signal on pad a is biased to the "on" state. Similarly, those signals will appear at output Ab and Bb if the control signal on pad b is biased "on." This is a double-pole, double-throw operation, as diagramed functionally in Fig. 5b. Note that because these are not just switches, but switchable FET's, the input signals are in all cases amplified before appearing at the outputs selected.

For the SP4T device shown in Fig. 6a, the signal gates in all four channels are interconnected and can be fed from either of two pads, A or B. The amplified input signal can thus be made to appear at any one of the four outputs (drains 1-4) by proper "on" biasing of the appropriate control gate (a-d respectively) using its pad. This single-pole, 4-throw operation is diagramed functionally in Fig. 6b.

All devices use 1 μm length gates, which were adequate for the initial work since it was at 10 GHz and below. Source-to-gate 1 spacing was kept as

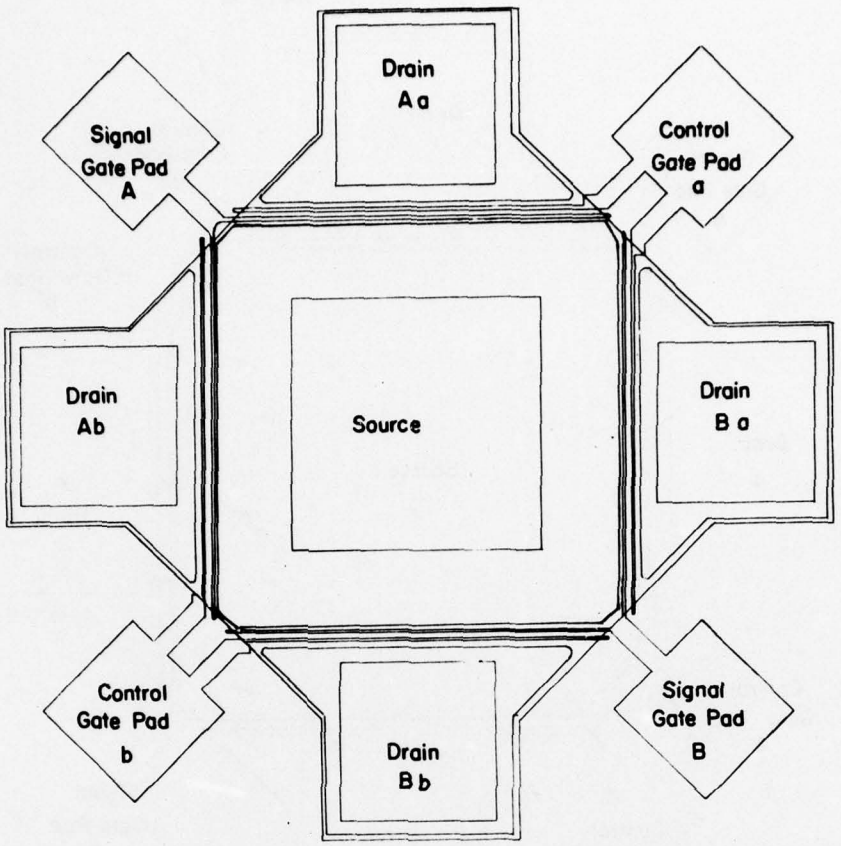

Figure 5a. Schematic Diagram of the DPDT Switch Device.

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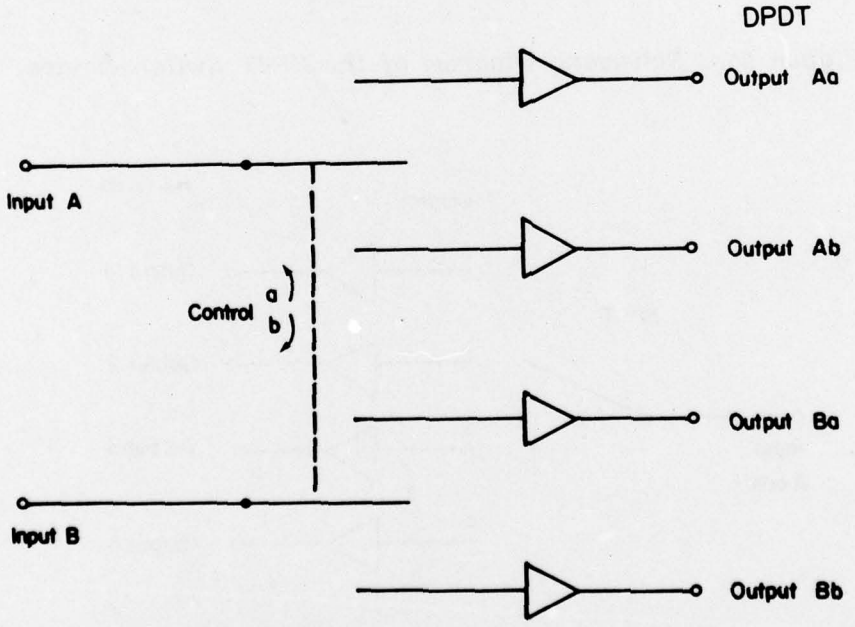


Figure 5b. Functional Diagram of the DPDT Switch Device.

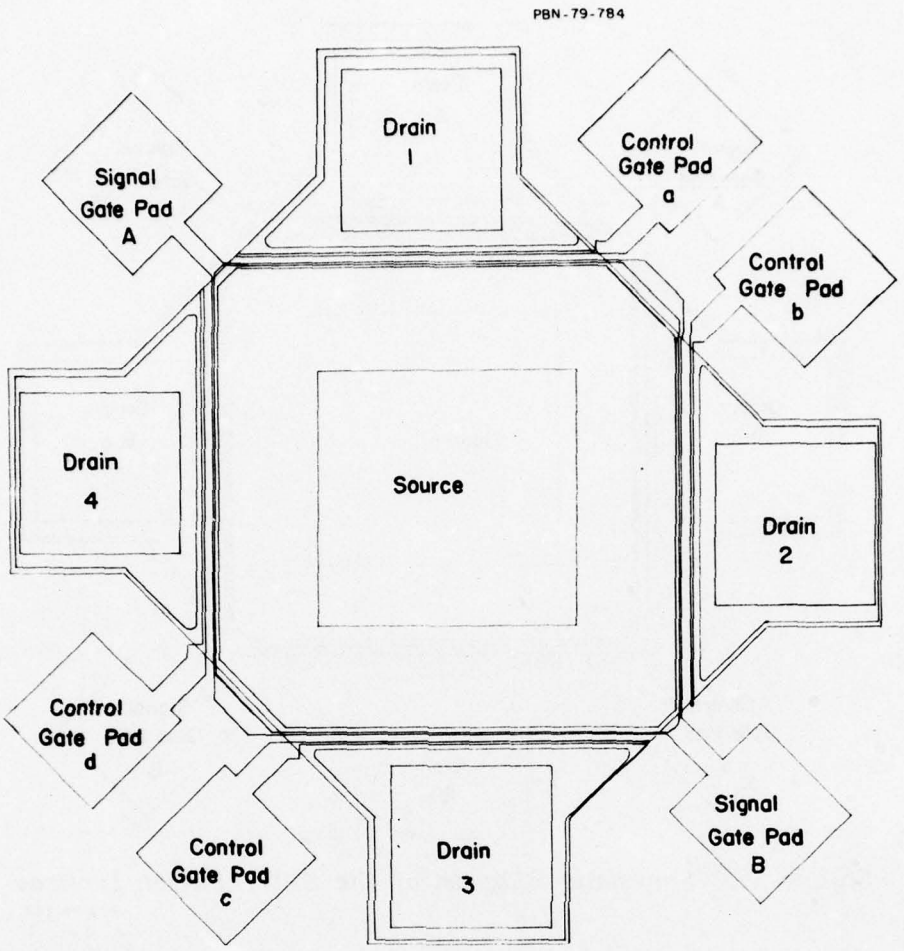


Figure 6a. Schematic Diagram of the SP4T Switch Device.

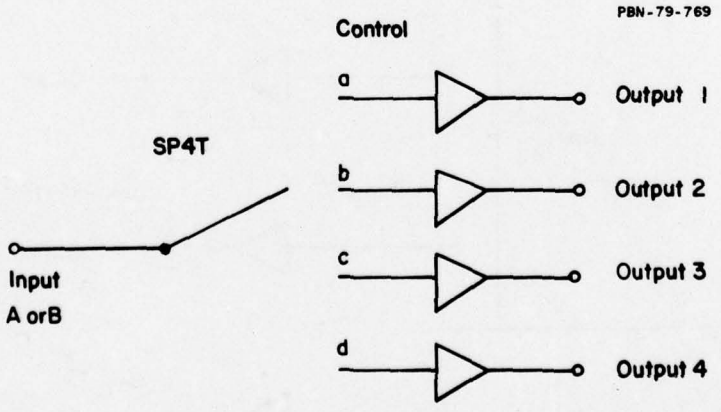


Figure 6b. Functional Diagram of the SP4T Switch Device.

small as practical ($\sim$ 1 μm). Intergate spacing was fixed at 2 μm. Initially, two types of devices were fabricated, those with a second gate-to-drain spacing of 2 μm, and those with a 4 μm space. Since no significant difference was observed between the two spacings, subsequent designs used only the 2 μm type.

2.2 Fabrication Technology

All devices were fabricated on material grown by vapor phase epitaxy on semi-insulating GaAs substrates. Normally, a three-layer structure, such as that shown in Fig. 4, was used. Here an undoped buffer layer separates the channel region from the substrate. The channel material was doped around 10^{17} cm^{-3} with thicknesses in the 0.3 to 0.5 μm range. The top layer was a heavily doped contact region with $n > 10^{18} cm^{-3}$ and $t \sim 0.2$ μm. A few of the early runs were made on material without this contact layer.

Figure 7 schematically outlines the processing sequence used for fabrication of these devices. Element isolation is achieved by a mesa etch into the channel layer followed by a multiple implantation of $^{16}O^{+}$ ions; this process isolates the off-mesa regions well into the buffer layer. Source and drain contacts are formed by a AuGe/Ni metallization which is alloyed into the contact layer, providing ohmic contacts with typical specific contact resistivities of less than 10^{-6} Ω cm^2. A recessed gate structure is used with Ti/Pt/Au as the gate metallization.

Low impedance source connections are made through the use of etched "via-holes." Evaporated metal followed by selective gold plating under the device area provides a low impedance connection to the backside ground, as shown in Fig. 7.

As part of the standard process, we are fabricating leads coming from all of the device's external pads (i.e., all pads but the source). These leads are plated gold and are designed in such a way that after wafer dicing one end of each lead extends beyond the die edge, where it can conveniently be connected to the test circuit or fixture. The chips have been diced either by scribing or by chemical etching.

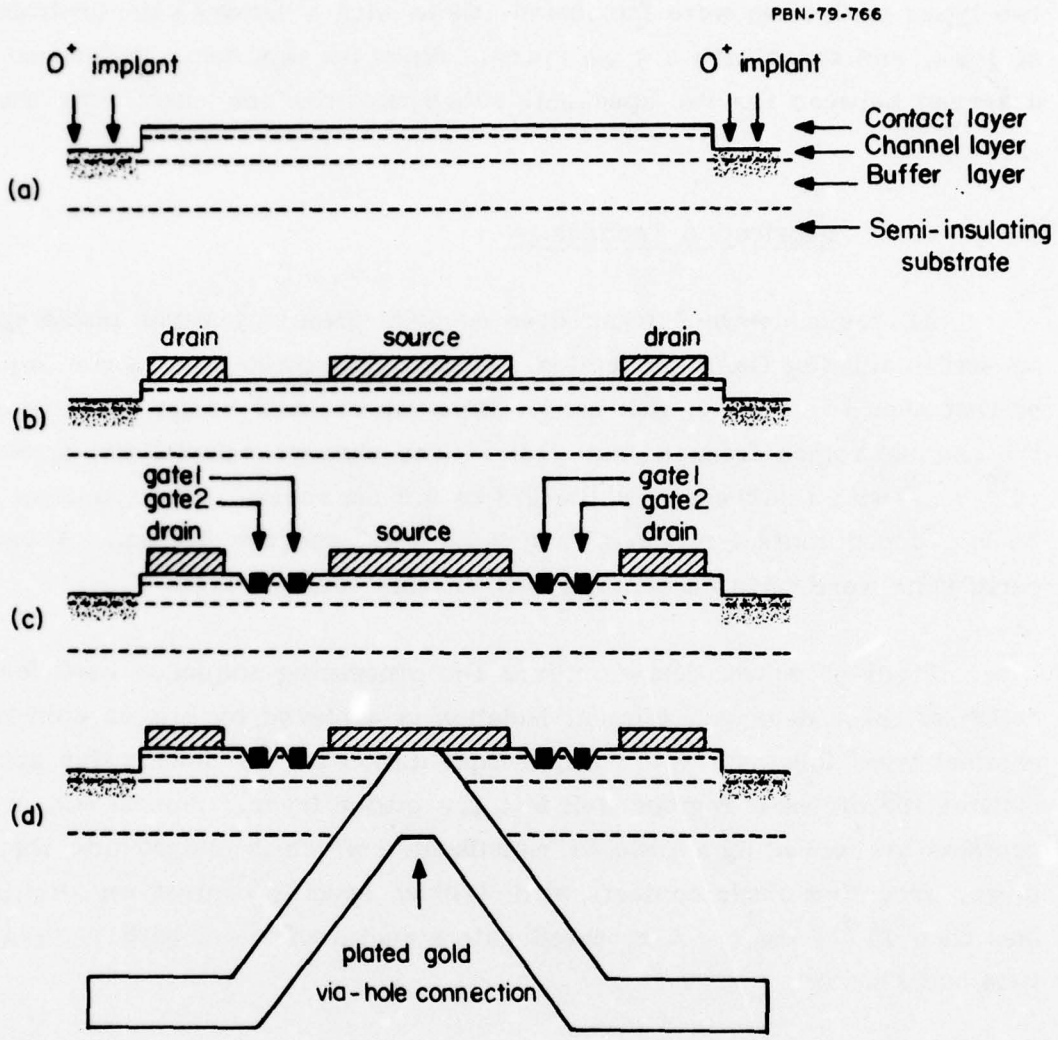


Figure 7. Dual-Gate FET Fabrication Process.

To date, 15 wafers have been processed into dual-gate switch devices. Of these, 13 have been completed with usable FET's on them. Table I gives a listing of these wafers.

TABLE I

DUAL-GATE FET SWITCH DEVICE WAFERS PROCESSED TO DATE

Wafer Number	Started	Completed	Stopped	(Reason)	Gate Metallization	Via Holes	Dicing
41716	05/30/78	06/13/78	.....	.....	Cr/Au	N	Scribe
41729B	05/30/78	06/13/78	.....	.....	Cr/Au	N	Scribe
82464	06/29/78	09/06/78	.....	.....	Cr/Au	N	Scribe
82465	08/14/78	09/21/78	.....	.....	Cr/Au	N	Scribe
82457	12/29/78	02/07/79	.....	.....	Cr/Au	Y	Saw
82585	12/29/78	.....	01/16/79	(Poor Gate Liftoff)	Cr/Au	...	...
72521	01/24/79	02/15/79	.....	.....	Cr/Au	Y	Saw
72523	01/24/79	04/02/79	.....	.....	Cr/Au	Y	Scribe
82639	03/09/79	05/01/79	.....	.....	Cr/Au	Y	Saw
82626	04/03/79	05/04/79	.....	.....	Ti/Pt/Au	Y	Scribe
82632	04/03/79	05/02/79	.....	.....	Ti/Pt/Au	Y	*
82635	05/21/79	07/10/79	.....	.....	Ti/Pt/Au	Y	Etch
82640	05/21/79	.....	06/11/79	(Poor Gate Liftoff)	Ti/Pt/Au	...	...
7A-57A	06/04/79	07/24/79	.....	.....	Ti/Pt/Au	Y	*
7A-57B	06/04/79	07/24/79	.....	.....	Ti/Pt/Au	Y	*

* *Dicing has not yet been done.*

3.0 DEVICE CHARACTERIZATION

The single most difficult problem in this contract has been how to characterize these complicated dual-gate structures. This applies whether the goal is measuring the I-V characteristics or the rf response. These switch structures have up to 9 independent ports (plus ground), which somehow must all be contacted in order to test the device completely. The situation is further complicated by the compact nature of the structure itself, which fits on an 18-mil square chip. Thus characterization of these structures required some rather novel test set-ups.

The problem divided itself naturally into two areas. The first was essentially dc characterization of the devices during and at the conclusion of processing. These measurements were done on the GaAs wafer as a whole rather than on discrete chips and consisted of I-V characteristics and the like. The other problem area involved the question of how to mount and interconnect discrete chips for microwave testing. Both of these areas will be covered in detail to illustrate the difficulties involved in handling multi-port structures.

3.1 dc Characterization

The dc characteristics of an FET device are important tools for monitoring the device fabrication process on the one hand and for indicating the ultimate rf performance on the other. Traditionally, such characteristics are obtained using some kind of wafer prober (usually manual) and a curve tracer. This method is satisfactory for looking at a few devices, especially if they are relatively simple.

The dual-gate structure is not simple in this sense. For example, one set of I-V curves will not suffice to completely describe the transfer characteristics of the device, as it will with a single-gate FET. The change of drain current at various drain voltages is now a function of <u>two</u> gate bias potentials. The multiport switch structures are four times more complicated, since there are four separate but interdependent channels to deal with in each device. For these structures, even the simplest set of I-V curves in which just one

drain and one gate bias are being changed require that 6 or 7 other pads on the structure be contacted and set to some predetermined potential. To start varying all the available parameters causes a geometrically increasing amount of data to be generated.

Having anticipated this kind of problem, we have been involved in an internally funded effort to develop a computer driven automated measurement system (AMS) capable of handling this kind of data acquisition task. The heart of the system is a Hewlett-Packard 9825 computer which acts as system controller. The computer drives a motorized wafer prober for bringing printed circuit cards with microprobe tips into contact with selected devices on a wafer. Signals fed through and measurements taken from these probes are also controlled by the computer. By automatically setting voltage and/or current levels at arbitrarily chosen points on the device and then measuring voltage, current, or capacitance at other points, the computer can acquire, through the AMS, all of the dc characteristic information required. These data can then be manipulated and presented in convenient printed or graphic form or stored for later use and evaluation. The system is even designed to look at a particular electrical parameter or set of parameters for every device on an entire wafer and deliver statistical or positional variation summaries of those measurements.

In the past year, we have been developing software for the AMS which will allow us to use the system on the dual-gate switch structures. Certain tasks are relatively simple, especially those directly related to device processing, such as channel saturated current monitoring during gate recess etching. These tasks have been implemented and the AMS is used routinely to do them.

The more complicated problems associated with detailed characterization of devices (I-V curves, transconductance, etc.) have not been fully implemented. An example of the part of the work that has been completed is shown in Fig. 8, which presents a series of I-V plots for a single dual-gate FET channel. The computer, using the AMS, was able to measure I_d while varying in a controlled fashion V_d, V_{g1}, and V_{g2}. The resulting information was then displayed

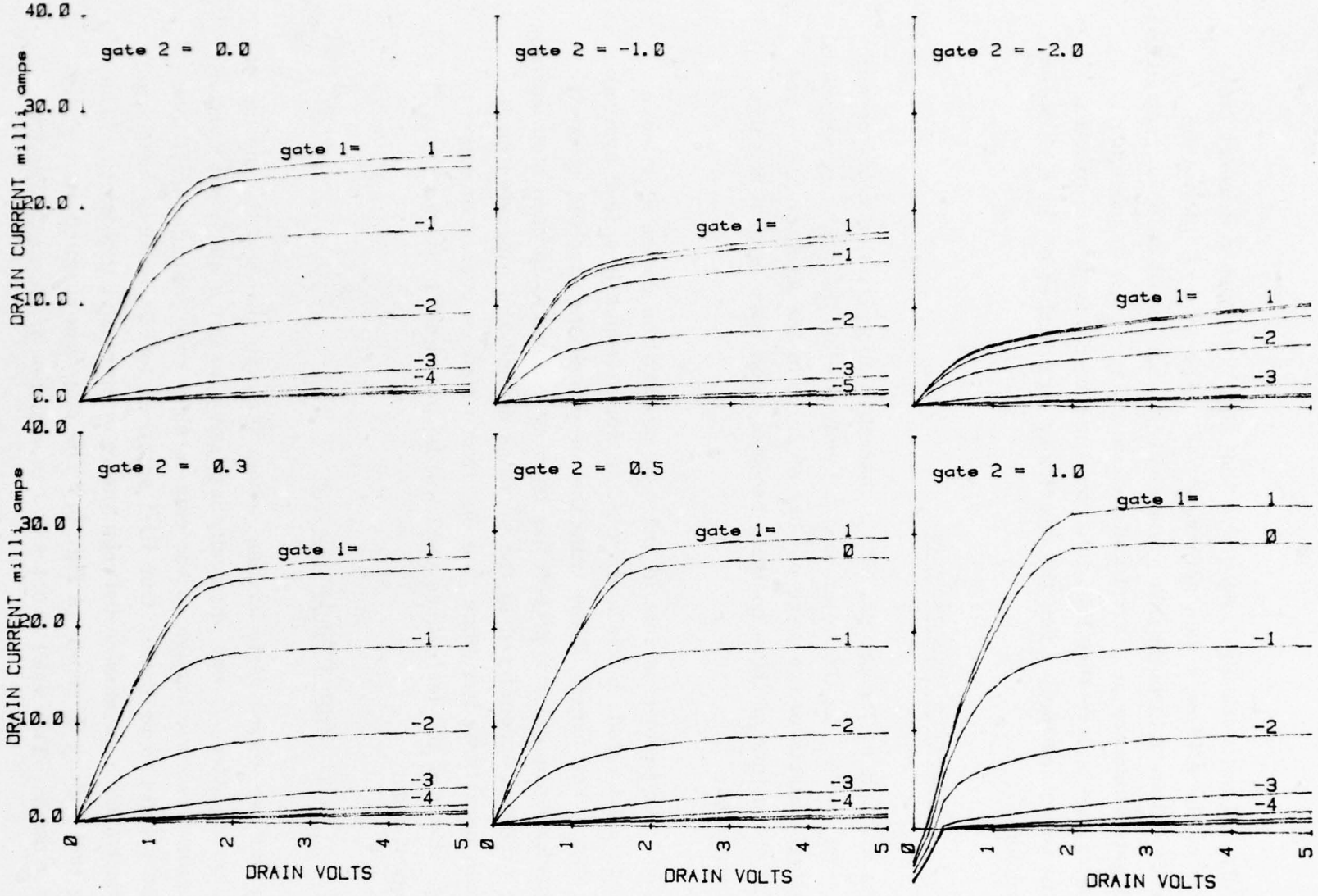


Figure 8. I-V Characteristics for a Dual-Gate FET Measured Using the AMS.

graphically, all automatically. We belive that this performance demonstrates the power of the AMS as a data gathering tool. The kind of information that can be obtained through this system will prove invaluable for understanding the dual-gate structure in general and the switch structure in particular. Furthermore, we believe that this data could not be obtained in a practical manner in any other way, given the complexity and number of the structures being studied.

3.2 Microwave Measurements

As difficult as the problem of dc characterization is, that of rf measurement is even worse. In the latter case not only are all the problems associated with getting contacts to the large number of ports in the small chip area the same, but the nature of those contacts becomes much more critical at microwave frequencies.

The basic problem is that in order to measure the device at rf some connection must be made between the outside world (which is a 50 Ω system) and the chip. The nature of the transition or transitions involved strongly affects performance. Our approach has been evolutionary, in each step learning from the problems encountered in the previous method and improving on it. There have been three iterations thus far from which an overall direction is emerging. Each of the techniques used will be presented in more or less chronological order.

3.2.1 Microstrip test fixture

It was recognized early on that, given the chip size and the number of ports to be contacted, it was physically impossible to get a sufficient number of 50Ω connectors close enough to the chip to allow some kind of direct interconnection scheme to be used. Our first approach to this problem was to put 50Ω microstrip lines on alumina between the connectors and the device. The resulting test fixture is shown in Fig. 9. The chip was mounted on a plated heat sink carrier. Two small ($\sim$0.1 × 0.3 in.) pieces of alumina were also

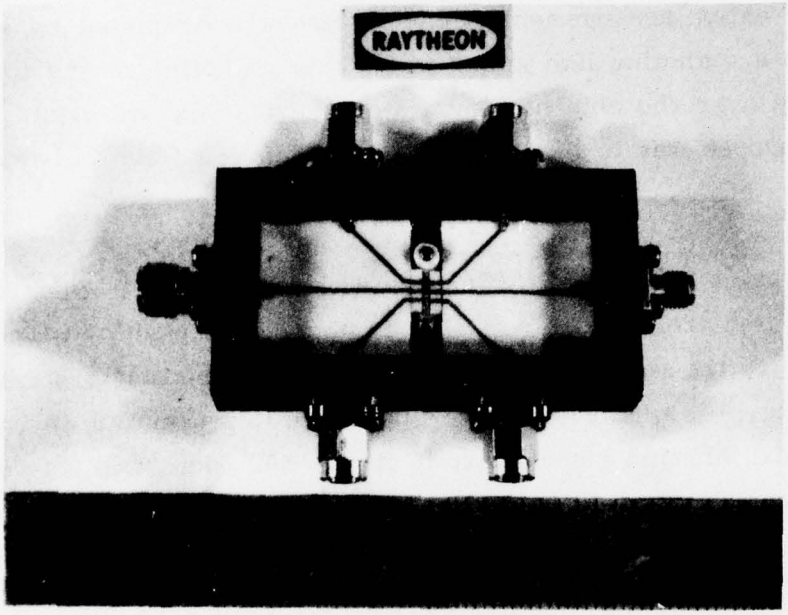


Figure 9. Microstrip Test Fixture.

mounted on the carrier adjacent to the chip. Each piece had printed on it 3 straight 50Ω line segments from which connections could be made to device bonding pads. The carrier was then placed between two 1 in. square alumina pieces on which were printed 50Ω lines connecting the ends of the straight line segments to six connectors arranged around the outside of the copper block which held the entire arrangement. The fixture was completed by a lid which was fitted with a guillotine-like structure. This guillotine nearly touched the surface directly over the chip and separated the test fixture cavity into two halves. Its purpose was to provide additional isolation from one side of the structure to the other.

There were a number of difficulties with this fixture. First of all, there are a total of three transitions from chip to connector, each of which can introduce error to the microwave measurements. The second problem is illustrated in Fig. 10, which is a close-up of the chip mounted on the carrier with the two small alumina pieces next to it. A 50Ω microstrip line on a normal 25-mil thick alumina substrate is nearly 25 mils wide. With a single device die size of only 18 mils square, it is impossible to get all 6 of these lines in close to the chip. Hence, the wire bonds between the device and the 50Ω microstrip are very long (10's of mils) and thus very inductive, providing another source of error in the measurements.

Yet another problem is the conflict between the device geometry and the fixture geometry. The device shown in Fig. 10 is a DPDT structure connected in a single-pole, double-throw configuration. In this arrangement, two drains and the signal gate pad between them are connected, along with both control gate pads. As can be seen, the drains are connected to lines on the bottom of the figure. In order to achieve maximum input-to-output isolation, the signal gate must be fed from the opposite side of the chip. To do this requires a wire bond which must cross over the active region of the device. This, in turn, can lead to unwanted feedback. In short, to connect any but the simplest configurations required wire bonds to cross near each other and near the device, leading to feedback and crosstalk problems.

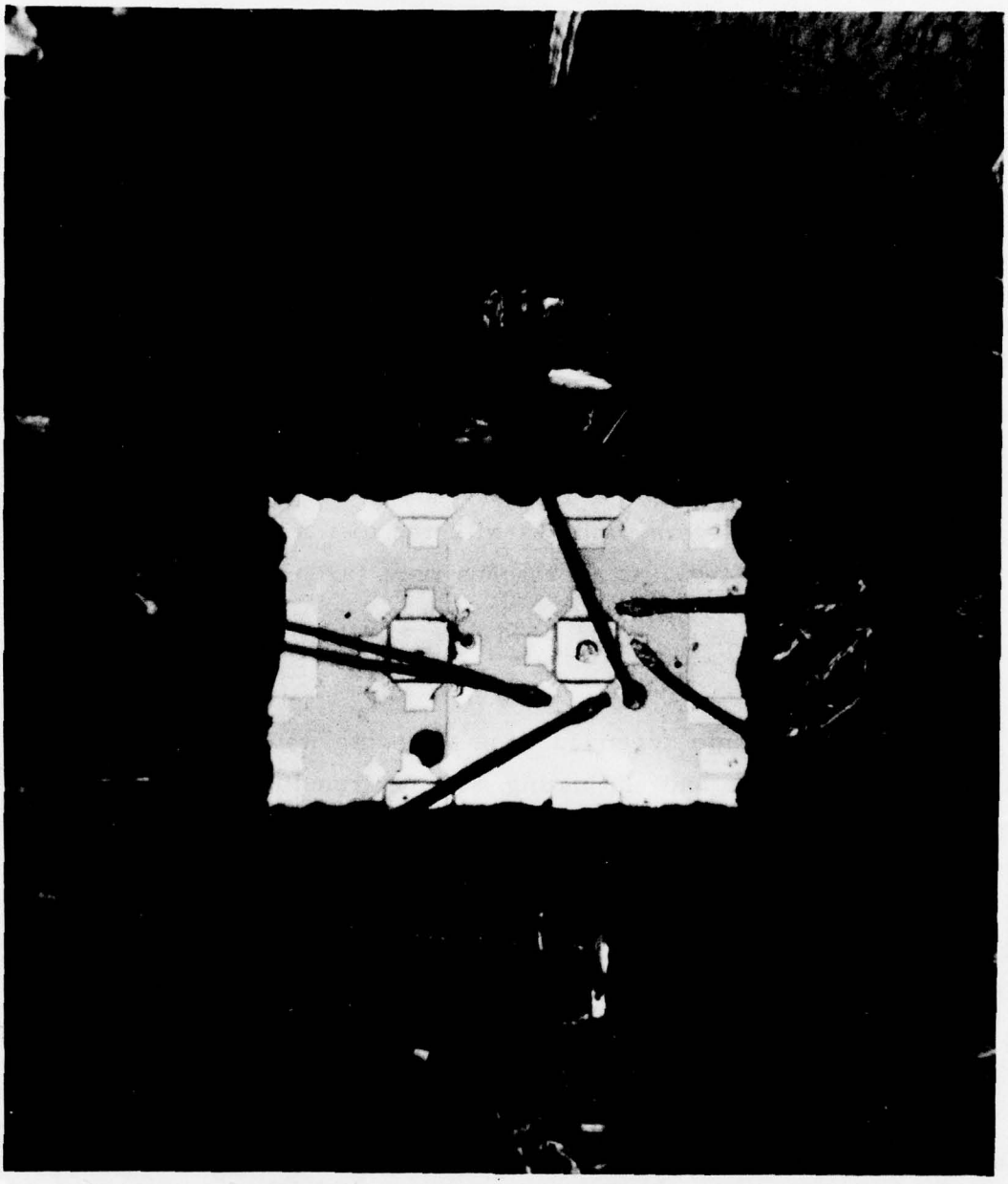


Figure 10. Double-Pole, Double-Throw Device Wired Into Microstrip Test Fixture as a Single-Pole, Double-Throw Switch.

One more drawback existed in this fixture. Even if the wire bonding could be managed, there were not enough lines to handle all of the signals needed to fully operate the device; thus some ports were always unterminated. These floating electrodes were one more source of feedback and crosstalk which tended to degrade the isolation and off-to-on gain ratio measurements. Furthermore, this type of fixture arrangement did not lend itself to the addition of more lines and connectors that would allow all ports to be terminated.

Despite all these problems we were able to use this test fixture for the necessary measurements. Both the simple SPST devices and the more complicated DPDT structures were studied, although in the latter case we were not able to test the device with all terminals connected, for the reasons described above. The results of these measurements are detailed in Sec. 4.0. The data did indicate that the devices would perform as predicted, but they also definitely indicated that there were problems with the test fixture, particularly regarding isolation. So two new approaches were taken.

3.2.2 Coaxial test fixture

Better measurements depended upon achieving well characterized terminals near the device and eliminating multiple transitions. As an intermediate step, we were able to modify a test fixture presently used for low-noise single-gate FET's. While this fixture could not be used for the multiport structures, it did allow good characterization of the simple SPST devices. This in turn increased our understanding of the basic dual-gate structure and gave us more confidence that the switch device would meet the ultimate performance goals.

The test fixture used had two coaxial connectors with tapered center conductors which brought the 50Ω input and output lines very close to the chip (Fig. 11). The chip was mounted on a carrier as before and connections were made from the signal gate and the drain on the SPST device to the input and output, respectively, of the fixture. A guillotine arrangement in the fixture cover directly above the chip carrier was again used to help isolate the two ports

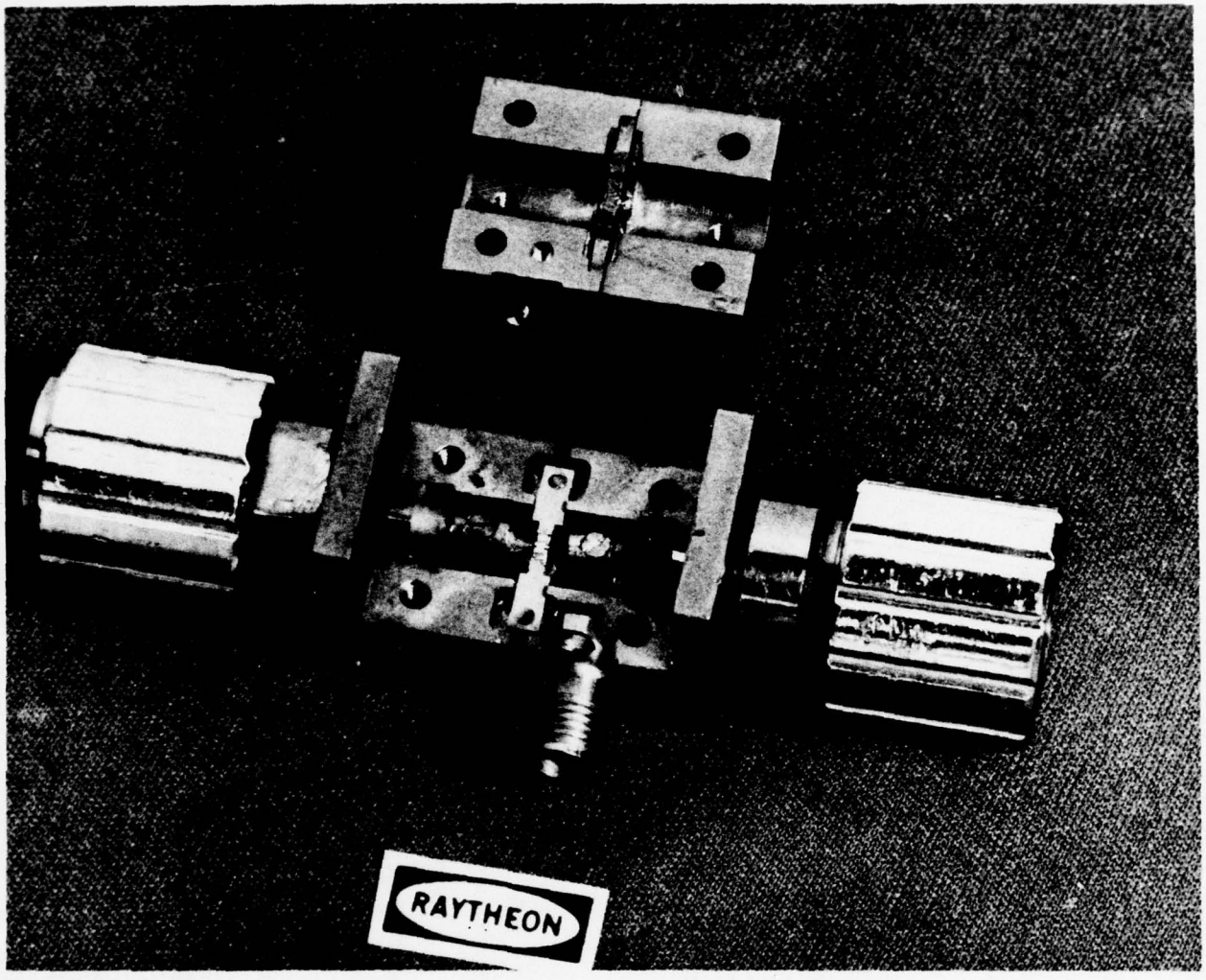


Figure 11. Coaxial Test Fixture.

by shielding them from each other.

A chip capacitor (∿10 pF) was mounted on the carrier adjacent to the device chip. A wire bond connection from it to the control gate pad was made. This bypassed to ground any rf signal on the second gate, allowing for simple dc biasing of the control gate. A bias wire between the capacitor and an external connector in the fixture side completed the mounting and interconnection process.

As will be shown in Sec. 4.0, the results of measurements made using this fixture were encouraging. They indicated that, when proper care was taken in arranging the connections of the chip to the outside, crosstalk and isolation could be reduced substantially, and that the intrinsic device performance thus measured was excellent. Now the problem was how to achieve these goals in a fixture capable of handling the multiport structures.

3.2.3 Coplanar line test fixture

We had learned thus far that, in order to get 8 or 9 ports in a single test fixture, the fixture must be large compared to the chip so as to accommodate the connectors. That, in turn, required some kind of long transition from the connector to the device, a transition which had to be kept as constant as possible and, ideally, identical for each port. The signal carrying medium, whether it was microstrip or coaxial line, had to be relatively large at the connector end (∿20 mils) to accommodate the connector center conductor and make a smooth microwave transition to it. Conversely, at the chip end it had to be small compared to the chip itself, so that many signals could be brought in close to the chip. These requirements eliminated microstrip, because its width is fixed by the substrate thickness for a given impedance level. Coaxial connectors were also eliminated, since they could not be readily tapered to a couple of mils in diameter and since they would also be excessively lossy at that size.

The coplanar waveguide seemed to be a possible solution to this problem which appeared to have many advantages over other methods. The coplanar

waveguide is a variation on microstrip in which the center conductor and ground planes are all on the same dielectric surface. The layout of such a structure is shown in cross section in Fig. 12. The general case of the coplanar line structure does not have an analytical solution for impedance. However, the specific case where $s_1 = s_2 = s$ does have such a solution, given by:

$$Z_o = \frac{1}{2\varepsilon_o c\sqrt{\varepsilon_r'}} \quad \frac{K(k)}{K'(k)} \tag{1}$$

where K and K' are the complete elliptic integrals and

$$k = \frac{\sinh\left[\frac{\pi}{2s}(b-a)\right]}{\sinh\left[\frac{\pi}{2s}(b+a)\right]} \tag{2}$$

The dielectric constant ε_r' is a function of the two separate dielectric constants ε_1 and ε_2. The form of the function is not known and had to be determined experimentally. Note that in this analysis the metal thickness t is assumed to be negligible compared with s, and d is assumed to be large compared with b-a.

The nice thing about coplanar lines is that the impedance is predicted to be strongly a function of the ratio of a to b and only weakly dependent on the value of a, the center conductor half-width, provided that $a << s$. Calculations based on formulas (1) and (2) showed that for s = 50 mils, a could range from 1 to 10 mils (center conductor widths of 2 to 20 mils) and Z_o could be held to within ± 2 percent of 50Ω, provided that the ratio of b/a remained fixed.

The coplanar structure thus provided a means of meeting the physical size requirements of the transition from the chip to the connector center conductors. It also offered other advantages. The ground planes between center conductors would offer some signal isolation. Those same ground planes offered a convenient place for grounding bypass capacitors used in the rf bypassing of the control gates. In fact, it would also be possible to ground the chip, and thus the device source, directly to the topside ground plane.

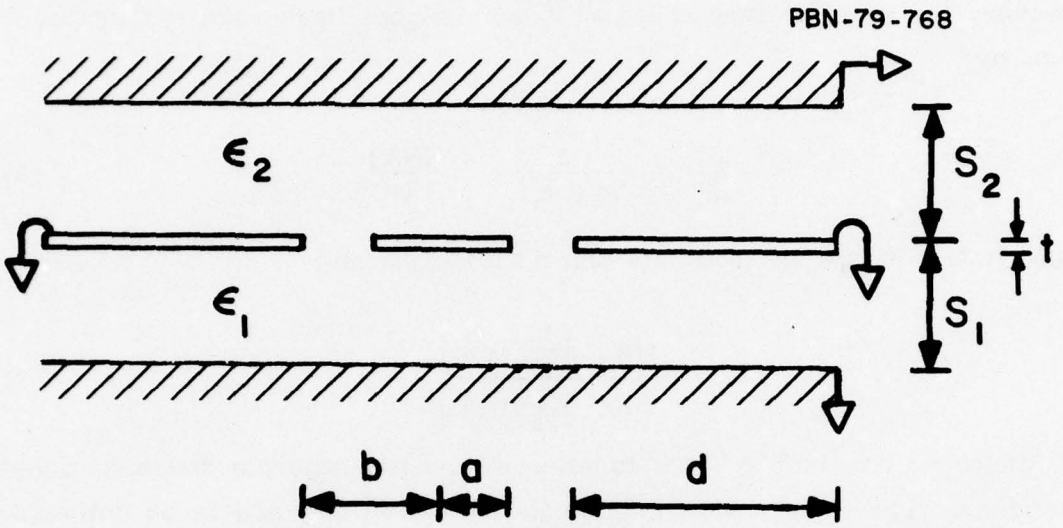


Figure 12. Waveguide Structure Coplanar Schematic Diagram.

The validity of the coplanar line analysis was not known, nor was the value of ε_r'. It was necessary to make some actual coplanar lines and measure them. Two structures were made with identical b/a values, having a center conductor width of 10 mils in one case and of 20 mils in the other. The alumina substrates were 50 mils thick, and the test fixture was machined with a 50 mil gap from the alumina surface to the top plate, assuring that $s_1 = s_2$.

The measured impedances of these two structures varied one from the other both quantitatively and qualitatively as the theory predicted. The form for ε_r' appeared to be simply $(\varepsilon_1 + \varepsilon_2)/2$. When this value was used, equations (1) and (2) predict $Z_0 = 51\Omega$ for the narrow line case versus a measured value of $51.0 \pm 0.5\Omega$ and a predicted $Z_0 = 49\Omega$ versus $50 \pm 0.5\Omega$ for the wider line. These results gave us sufficient confidence to proceed with the coplanar line test fixture idea.

The alumina circuit we are using for the coplanar line test fixture is shown in Fig. 13. The chip is mounted in the center of this circuit. There are six coplanar line center conductors surrounded by ground plane metallization. They are flared from 3 mils in width at the chip to 20 mils at the edges, where the connector center conductors make pressure contact to the lines. The four lines coming in from the sides are for the four output signals (one from each drain). The lines coming from the diagonals line up with the signal gate pads. On the opposite diagonals near the chip there is room to mount up to four chip capacitors (10 pF each), two on each corner. These can be used to bypass up to four control gates, whose pads are on these two corners of the device. From each capacitor, a lead is connected to one of the narrow lines going diagonally away from the chip and toward one of the large (40 × 40 mil) pads located near the corners of the alumina. These pads provide the control gate dc bias connection points. They are contacted by means of spring-loaded pins precisely positioned and mounted in the test fixture top plate. The test fixture itself is shown in Fig. 14.

The substrates are 50-mil thick alumina, plated with 6 μm of gold on the bottom. A thin TiAu layer is deposited on the top, after which the structure is defined in photoresist and plated to 6 μm. The thin metal is

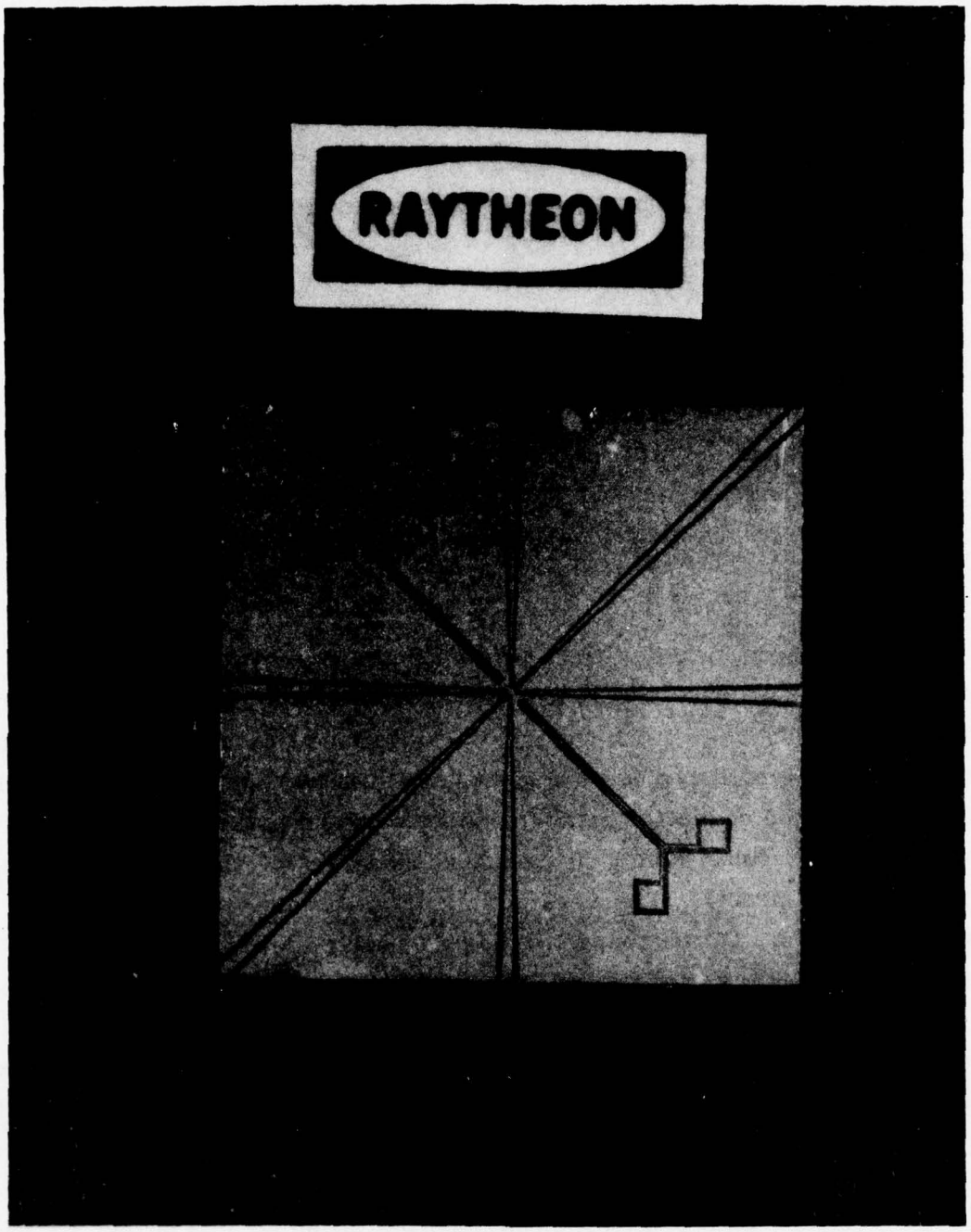


Figure 13. Alumina Coplanar Circuit.

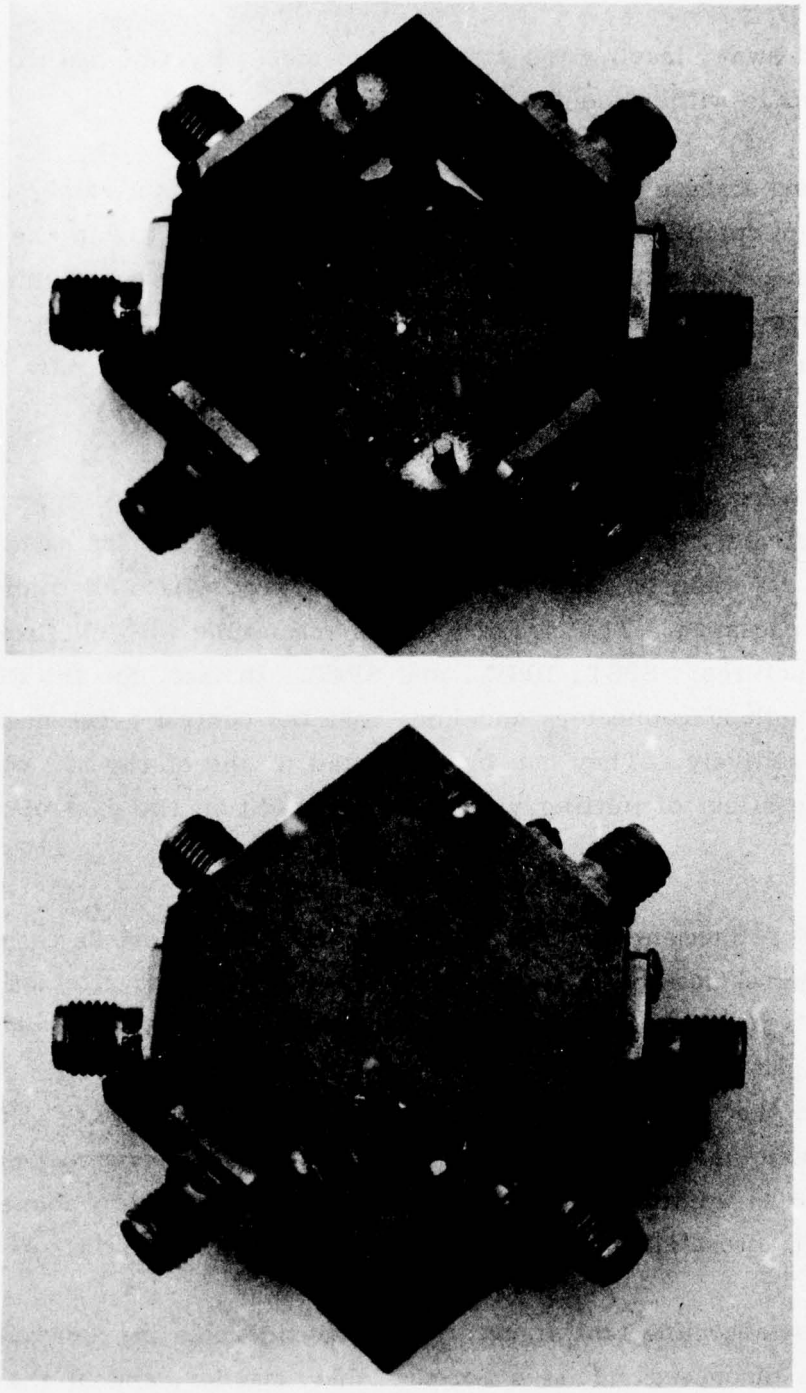


Figure 14. Coplanar Line Test Fixture.

finally etched away, leaving the completed circuit. By this method dimensions are maintained to within about 0.1 mil.

The test fixture has six SMA connectors for the six rf signal lines. There are four spring-loaded Pylon Pogo Contact connectors in the top plate for bias feeding the control gates. There are 50-mil spaces machined into the top plate above the coplanar lines to maintain $s_1 = s_2$. Elsewhere the clearance between the cover and the circuit is minimal to help break up any cavity resonances that might exist at the frequencies of interest.

In practice, the chip and the necessary capacitors are epoxy mounted onto the substrate. The necessary wire bond connections are made and the whole circuit can then be placed in the test fixture, where all connector contacts are made by pressure. The circuit itself is compatible with all three types of switch structures: SPST, DPDT, and SP4T. In fact, for the SPST chips, there are enough rf connectors and lines that the control gates need not be bypassed capacitively. They can be connected to one of the 50Ω coplanar lines, and the effect of putting various tuned loads on the control gate can then be studied.

A final refinement involves modifying the switch devices themselves. By using the integral beam lead technology described in Sec. 2.0, leads from each of the device's pads can be fabricated during processing. After dicing, if the leads are properly arranged, they will extend over the chip edge and line up precisely with the various coplanar lines and bypass capacitors. This allows a simplified bonding procedure which is at the same time more precise and more reproducible. In addition, without the wire bonds looping up above and over the chip itself, crosstalk between ports should be reduced still further.

The coplanar line test structure is a considerable improvement over the other methods discussed. It is a more reliable, simpler, and at the same time more exact means of embedding the device in a well-characterized testing environment. It is also an important intermediate step for the all-monolithic test structure toward which we are striving.

4.0 MEASUREMENT RESULTS

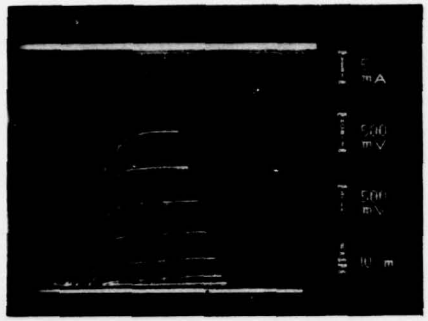
This section is primarily concerned with the results of the rf measurements. However, the dc device characteristic measurement results will be briefly described, especially as they relate to the rf data.

4.1 dc Measurement Results

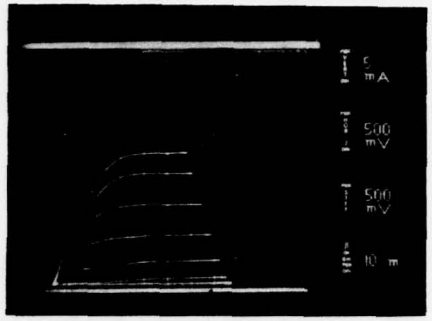
For reasons explained in the previous section, dc characterization of the dual-gate switch devices was necessarily limited. Without a fully operational AMS, detailed measurements of large numbers of devices were not possible. In general, what measurements were done were limited to spot checks of several devices on a wafer to assure that at each step in the processing they conformed closely to target values that had been set for each parameter. The I-V characteristics shown in Fig. 15 are typical of the kind of data taken and are representative of the devices from most of the wafers processed thus far.

As can be seen from these data, the devices had pinch-off values of around -2 V. The saturated currents were about 25 to 30 mA. Here saturated current is defined in the usual way as far as gate 1 and drain bias conditions are concerned. The gate 2 bias is set as far forward in the positive sense as possible without drawing significant ($\geq$ 1 mA) forward injection current. This is usually about +2 V. The dc transconductance at maximum gate 2 bias for gate 1 grounded was in excess of 15 mmhos.

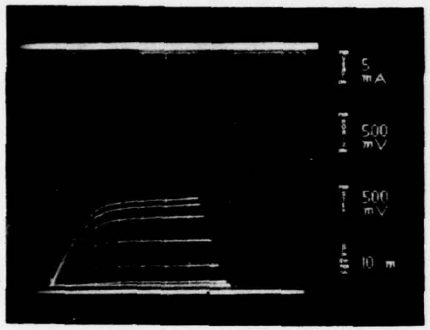
The kind of dc results that were particularly revealing with respect to rf performance are shown in Fig. 16. These pictures show the I-V characteristics under identical conditions for the four separate channels defined by a single SP4T switch device. The interesting feature is that while only very slight differences in I_{DSS} are seen between the top and bottom channels or the two side channels, the variation between adjacent, orthogonal channels is substantial (> 10 percent). This effect shows up in the microwave results, as will be seen later. It can also be observed in the relative variation in pinch-off



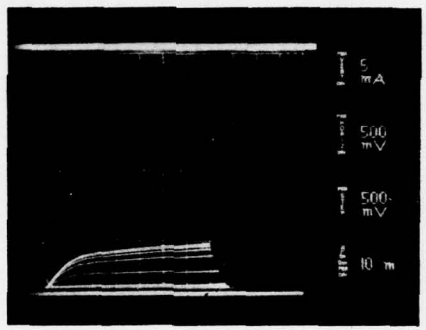
V_{g_2} = +2.0 V



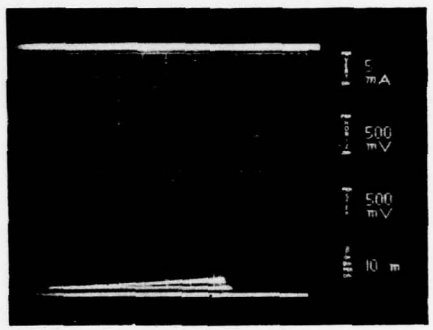
V_{g_2} = +1.0 V



V_{g_2} = 0 V



V_{g_2} = -1.0 V



V_{g_2} = -2.0 V

Figure 15. Single-Pole, Single-Throw I-V Characteristics.

V_{g_1} = +0.5 to -2.5 V

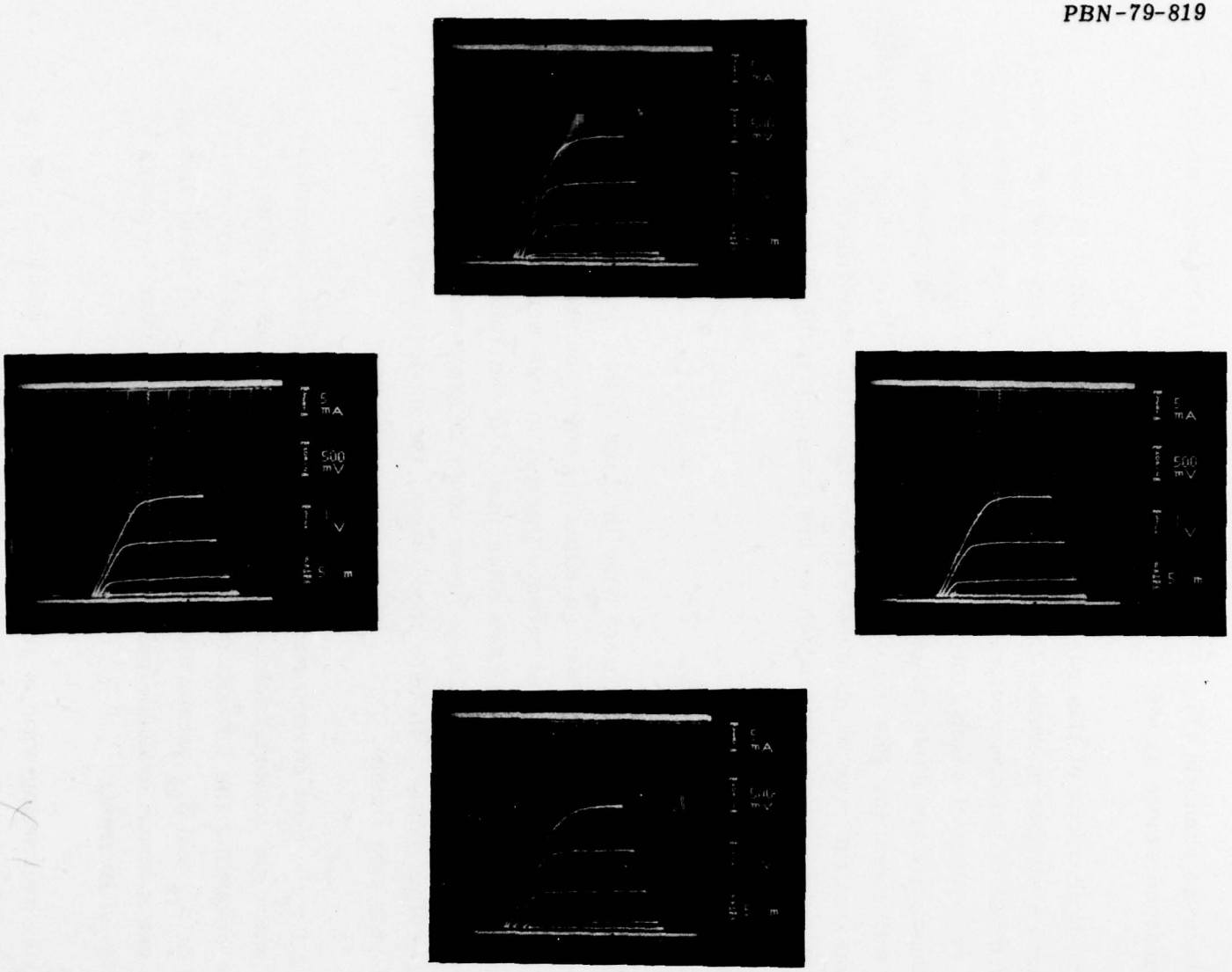


Figure 16. Single-Pole, Four Throw I-V Characteristics.

V_{g_1} = +0 to -3 V

V_{g_2} = +2.0 V

voltages between channels (Fig. 17). This variation was, of course, reflected in the transconductance as well.

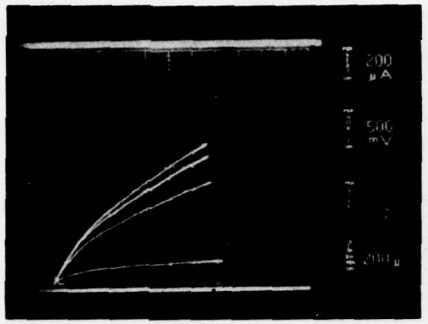
The implications of this variation are significant in that it is important for balanced switching operation that the four channels in this case have very nearly identical rf performance, so that uniform gain and phase response can be expected regardless of which "throw" of the switch is chosen. The reasons for the anisotropy are likely related to our channel recess etch process. Understanding and correcting this problem requires the kind of large-sample statistical information that can only be obtained with an automated measurement technique. That is, of course, the method which we are presently using to investigate this problem.

4.2 Microwave Results

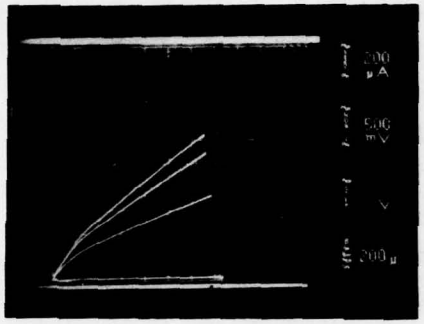
Microwave measurements were done in three ways. Initially, the gain and noise figure were measured on an automatic noise analyzer system. However, as the gain and isolation were of primary interest in this work and the noise figure decidedly secondary, we more often used a direct tuned power gain set-up in which the calibrated input power could be compared directly to the measured output power. In both these cases, the devices were tuned using coaxial double slug tuners.

By far the most common means of measuring microwave performance was with our automatic network analyzer. This equipment afforded us an easy method of observing the forward (S_{21}) and reverse (S_{12}) gain, as well as the variation of S_{11} and S_{22} versus changing bias conditions. We could also automatically get maximum available gain and stability factors over the range of frequencies of interest.

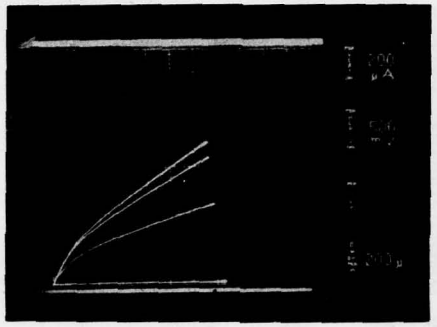
After overcoming some of the very early mounting, bonding, and test fixture problems described previously, the first single-channel dual-gate FET results were made in the microstrip test fixture on SPST devices from wafer 82464. The best results obtained were 14.3 dB gain with 3.6 dB noise figure



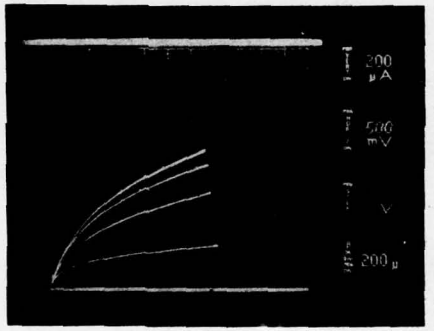
V_{g_2} = -3.15 V



V_{g_2} = -2.54 V



V_{g_2} = -2.47 V



V_{g_2} = -3.21 V

Figure 17. Single-Pole, Four-Throw V_p Characteristics.

V_{g_1} = +0 to -3 V

at 4 GHz, and 7.2 dB gain with 5.3 dB noise figure at 10 GHz. In both cases, the maximum gain and minimum noise figure points were fairly broad and corresponded to roughly the same bias and tuning conditions.

The poor performance was due to a number of factors. First, the problems involved with the test fixture played a role, as described in the previous section. Second, the bias conditions (V_D = 3.5 V, V_{g1} = -0.5 V, V_{g2} = + 1V) were probably not truly optimum. Experience has subsequently shown that the maximum gain is obtained for $V_{g2} \lesssim 2$ V and $V_{g1} \gtrsim 0$ V. However, the conditions used in this case were the best that could be achieved for stable device operation. Finally, the chips from the wafer were not "via-hole" grounded. Consequently, a rather long and thus inductive source beam lead had to be used to ground the source pad. This undoubtedly degraded device performance.

At this time, the isolation and hence the stability of the device were improved somewhat by introducing the guillotine into the test fixture top plate. Network analyzer results of the maximum gain for the condition that $S_{12} = 0$ and for V_D = 2 V, V_{g1} = -1 V and V_{g2} = 0 V are shown in Fig. 18. The *off gain* (V_{g2} = -2 V) was measured, and the on-off gain ratio [Gu_{max}(on) - Gu_{max}(off)] is also plotted in Fig. 18. In both cases the gain versus frequency dependence shows the expected 6 dB/octave and 12 dB/octave behavior, respectively. The dip in the gain and isolation at the high frequency ends of the curves are not, we believe, intrinsic to the device but reflect the effects of the combined problems of bonding, microstrip transitions, and cavity resonances of this test fixture on port-to-port isolation.

Via-hole source grounding significantly improved both the gain and stability of the next batch of devices measured. Figure 19 shows the on and off gain of a SPST device from wafer 72521 under the bias conditions of V_D = 4V, V_{g1} = 0.2 V and V_{g2} = 2.0 V. Notice that, with the low inductance via-hole grounding, the device is now stable enough to be biased at what proved to be, as expected, optimum conditions. The maximum available gain appears to be greater than 10 dB up to 10 GHz, with on-off isolation of about 36 dB across the 5 to 10 GHz band. Again, the results near 10 GHz are odd,

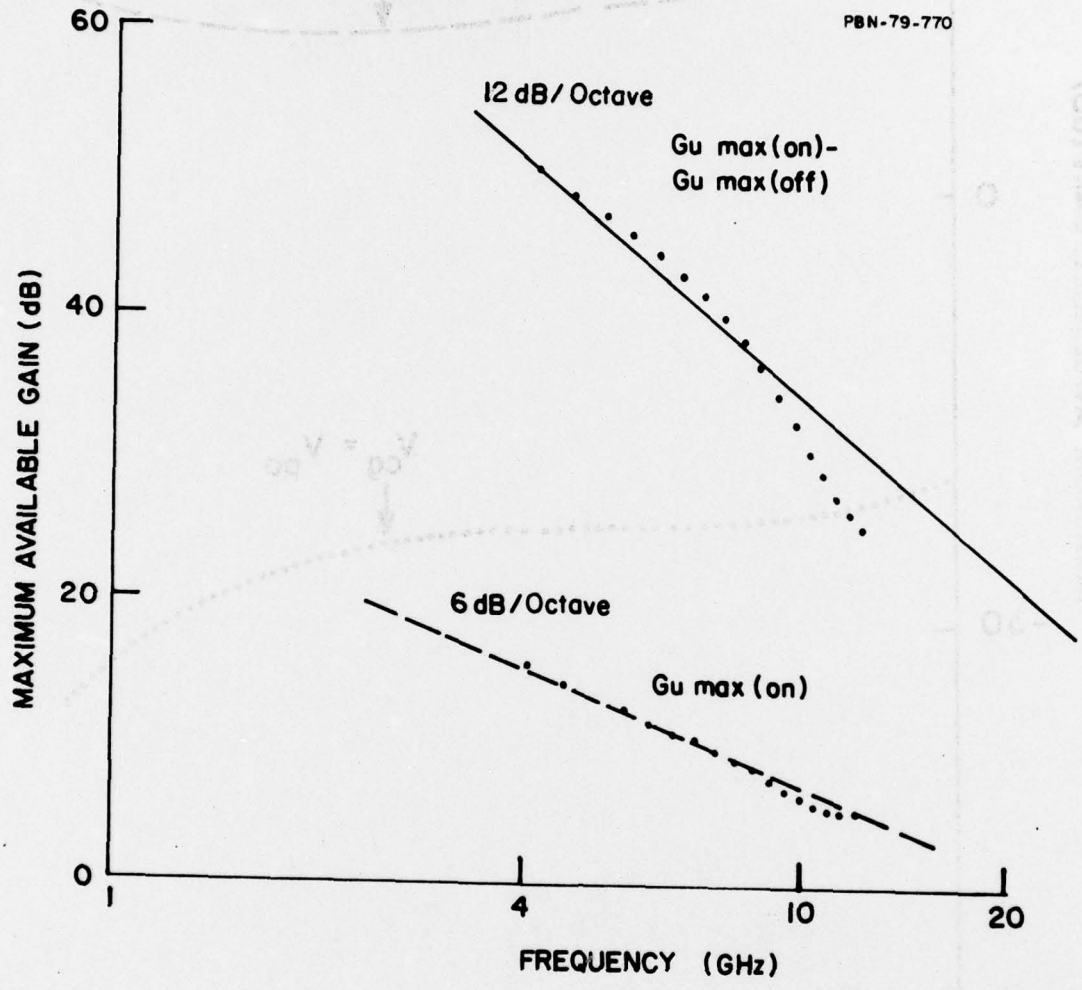


Figure 18. Maximum Available Gain and On-Off Gain Ratio for a SPST Device.

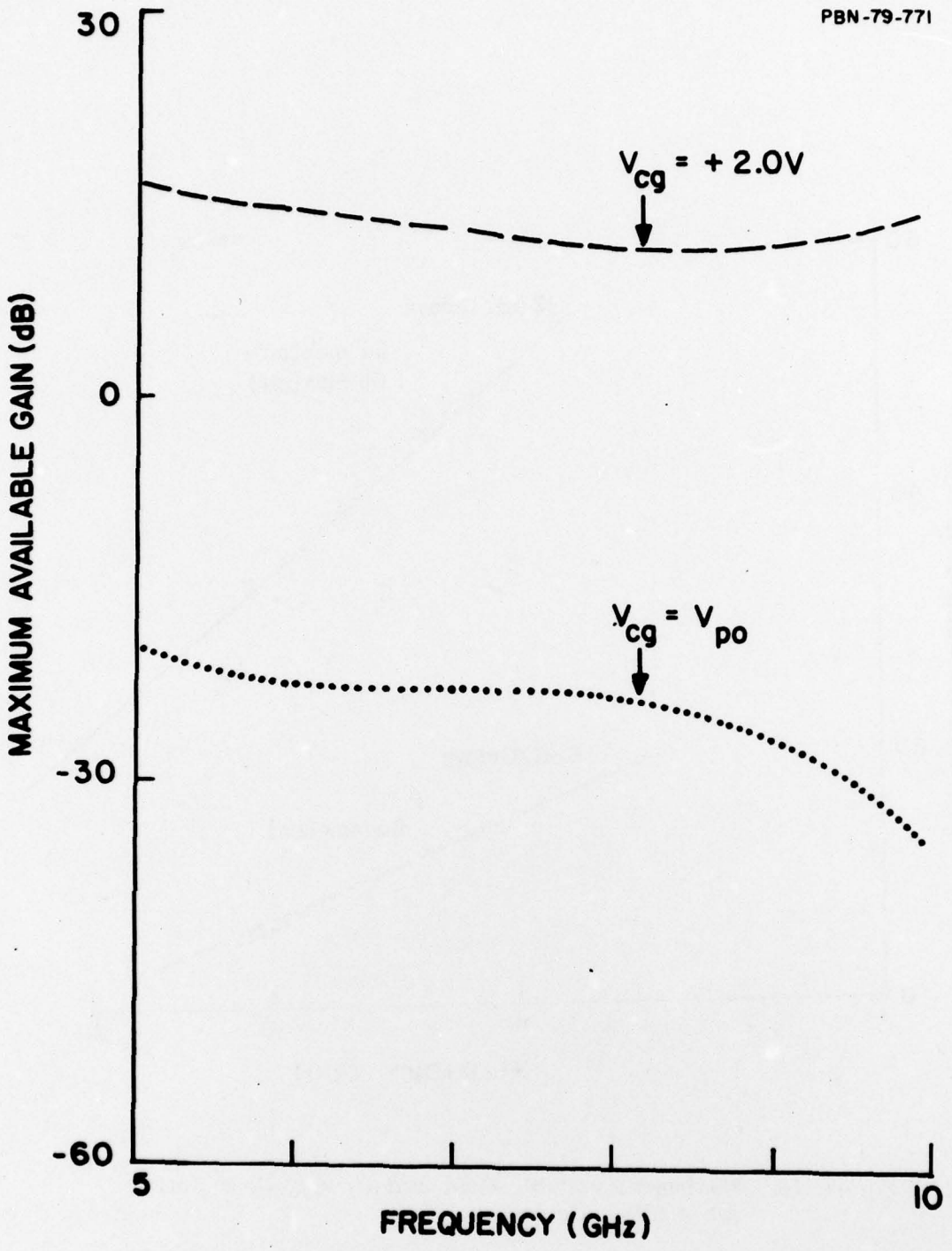


Figure 19. SPST Device, Output Varying Control Gate Voltage

V_D = 4.0 V

V_{sg} = 0.2 V

apparently still due to the fixture. But the data indicate that the dual-gate structure at least has the potential for high gain and good isolation.

At this point we attempted to look at the switch structures as switches for the first time. A chip from wafer 82457 was mounted and bonded as shown previously in Fig. 10. As discussed in Sec. 3.2.1, because of the insufficient number of signal lines and the problems involved in connecting to the device, the full DPDT structure could not be tested but rather only a single-pole, double-throw portion of it. The other ports had to be left floating, with the inevitable problems that this condition caused. Nevertheless, this configuration still allowed a number of key experiments to be performed.

First, a direct comparison of the output of these two orthogonal channels under identical conditions is possible. This is done by setting both drain biases and control gate biases the same. Since the signal gate is common to both channels, it is a priori identical in the two channels. The output gain can then be examined at each drain. The results (Fig. 20) show a uniform difference of about 1.5 dB over the frequency band. The dc transconductance variation between channels (reflected in the typical I_{DSS} and V_{po} variation seen in the dc characteristics in Sec. 4.1) is in the right direction and is the right magnitude to exactly account for this shift. This clearly illustrates how the variation in the dc characteristics between orthogonal channels is reflected in their subsequent rf performance and why that variation is significant and must be corrected.

In Fig. 21, we are examining the output of channel 1 while channel 2 is turned on ($V_{cg2} = 0$) and then off ($V_{cg2} = V_p$) in order to study crosstalk effects between two channels sharing a common signal gate. The effect is small (1 dB or less) but undeniable, and we have no explanation for it at present. We feel, however, that what crosstalk effects are evident in this data are most likely due to external factors (e.g., wire bonds) rather than intrinsic to the device, and we hope to demonstrate this with the improved coplanar line test fixture.

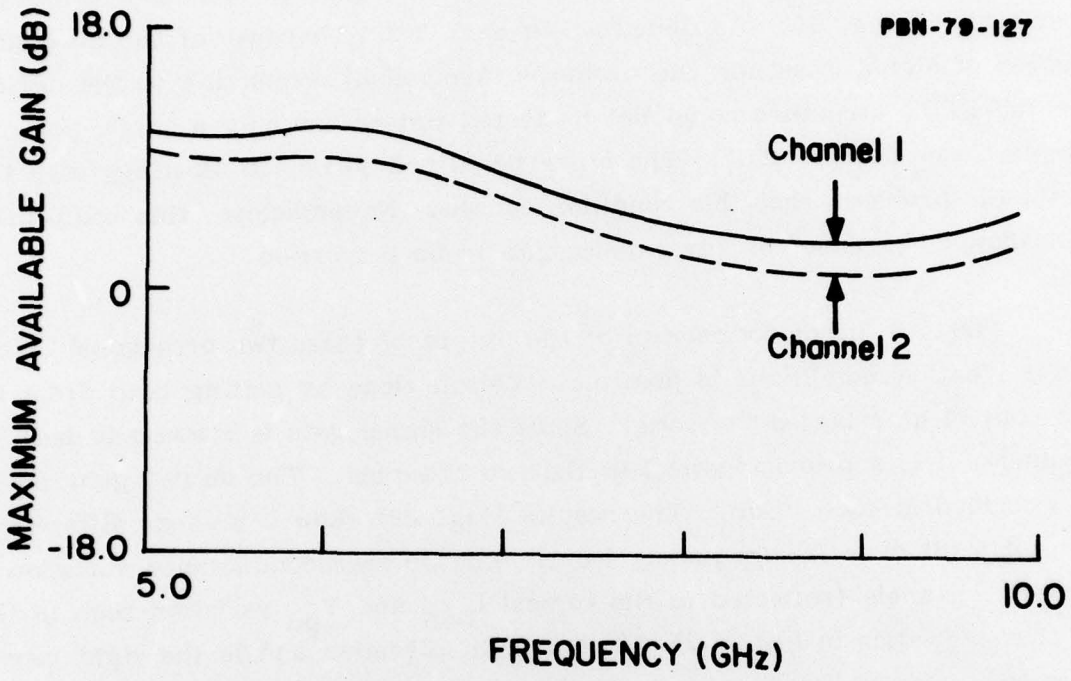


Figure 20. Channel 1 Output Vs. Channel 2 Output.

$$V_d = 2.5\ V$$

$$V_{sg_1} = V_{sg_2} = -0.8\ V$$

$$V_{cg_1} = V_{cg_2} = 0\ V$$

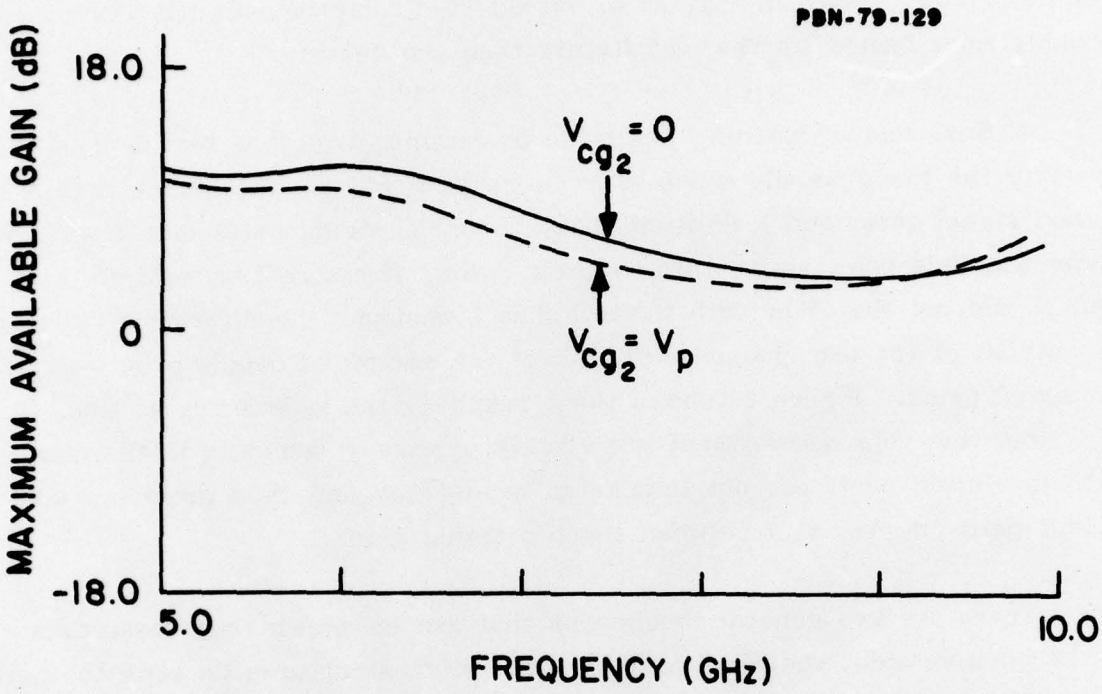


Figure 21. Channel 1 Output Varying Channel 2 Control Gate Voltage

$$V_d = 2.5\ V$$
$$V_{sg_1} = V_{sg_2} = -0.8\ V$$
$$V_{cg_1} = 0\ V$$

Another way to study crosstalk effects is to turn on and leave on one channel (in this case no. 2) and look at the on-to-off ratio of the other channel to see how much coupling there is between the two outputs. The results of this measurement are shown in Fig. 22 to exceed 20 dB, again a figure which is probably more limited by the test fixture than the device.

A final test of isolation was made by reconfiguring the test device. By using the two channels which share a common control gate rather than a common signal gate, and looking at those channels' signal gates and drains, we realize a double-pole, single-throw switch. Now, if a signal is fed into one channel and not the other with the switches biased on, the difference between the outputs of the two channels will reflect the amount of coupling between the two signal gates. Figure 23 shows these results; the isolation is at least 15 dB. Note that this measurement is probably especially sensitive to the fact that the unused ports are not terminated in any way and thus provide a convenient path for crosstalk between the two signal gates.

There are two general conclusions that can be drawn from these data. On the positive side, they indicate that the switch structures do seem to operate as switches. There is a substantial amount of gain and, more important, there does not seem to be a substantial amount of crosstalk, especially crosstalk intrinsic to the device. On the negative side, the conclusion is that this arrangement for testing these structures is woefully inadequate. It is a cumbersome approach, too limited in scope and flexibility to handle the most complicated of the switching functions. The character of the results, particularly at the higher frequencies, indicates basic problems inherent in the fixture structure, limiting the accuracy and sensitivity of some of the most critical measurements. It was these factors which eventually drove us toward the monolithic test structure idea and the initial step along that course, the coplanar line test fixture.

While designing the coplanar test fixture and the new mask set for the chips to go with it, we made one more attempt to demonstrate that, given good input-to-output isolation and reasonable chip-to-test fixture transitions, we

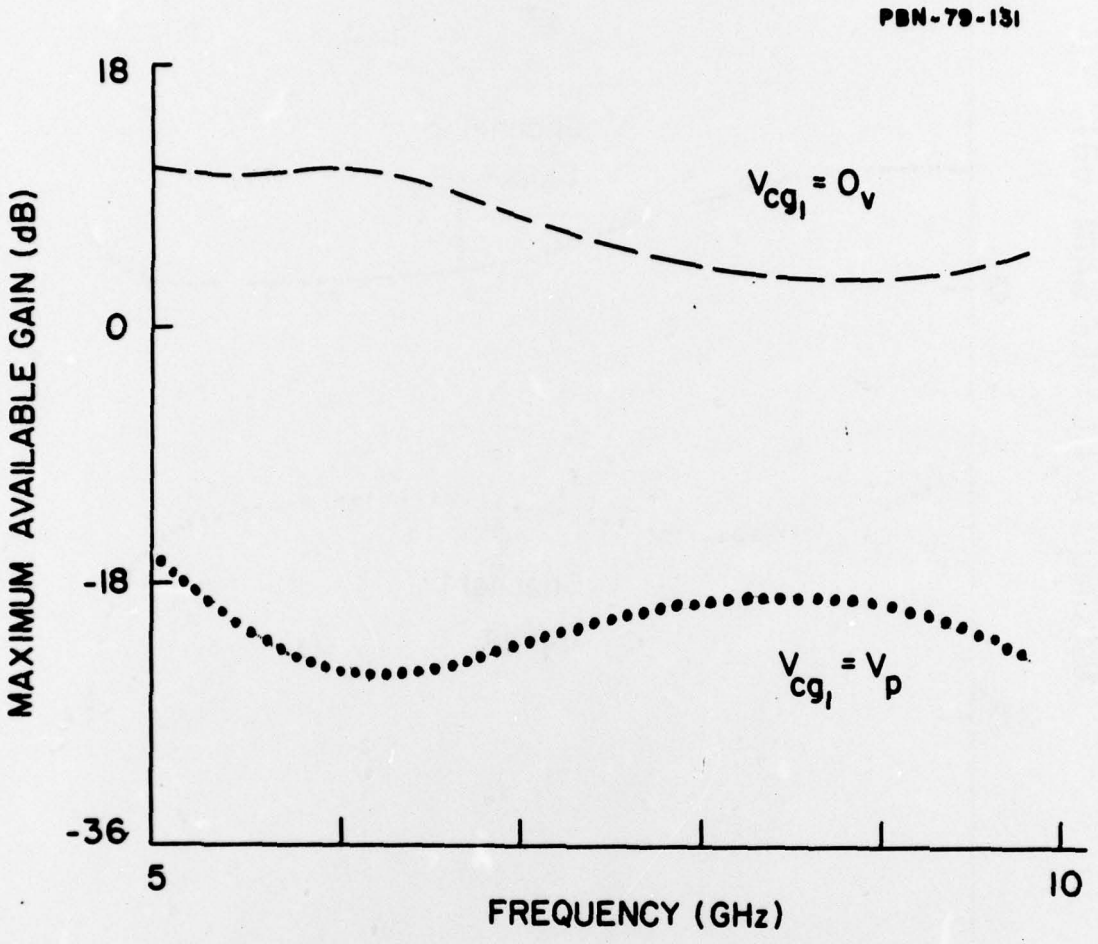


Figure 22. Channel Output Varying Control Gate 1 Voltage

$$V_d = 2.5\ V$$

$$V_{sg_1} = V_{sg_2} = -0.8\ V$$

$$V_{cg_2} = 0\ V$$

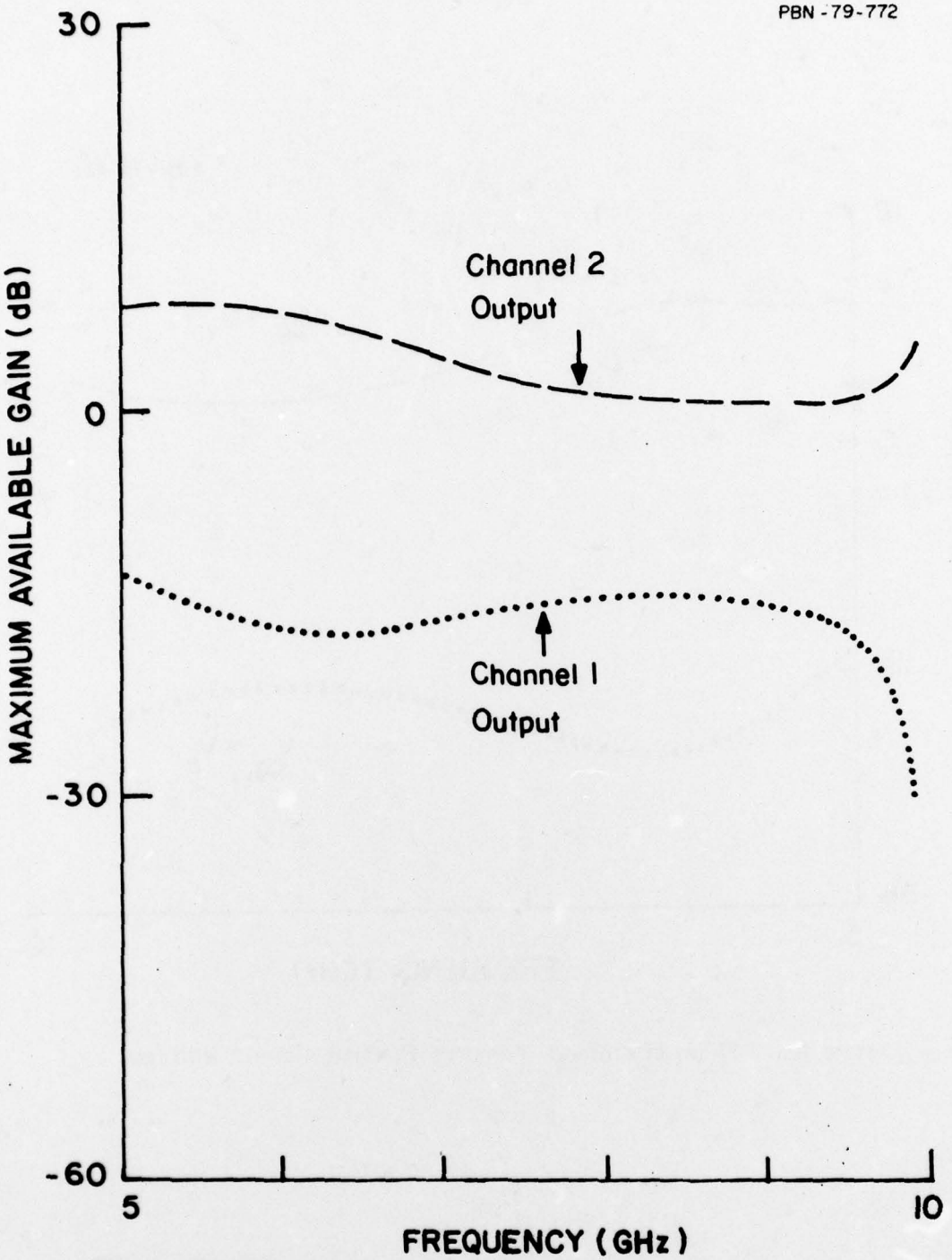


Figure 23. Channel 2 Output vs. Channel 1 Output with No Signal on Channel 1 Input.

$$V_d = 2.5\ V$$
$$V_{sg_1} = V_{sg_2} = -0.8\ V$$
$$V_{cg_1} = 0.0\ V$$

could achieve state-of-the-art dual-gate FET performance. We were finally able to do this using the coaxial test fixture described in Sec. 3.2.2.

SPST chips from wafer 82626 were mounted in this fixture and measured in the coaxial power gain set-up. The power gain as a function of input drive was measured for small input drive conditions ($\leq$0.1 mW) and the linear gain region was found. This was done for several different control gate bias values to examine the on-off ratio of the device. The results for the two (orthogonal) channels of an SPST chip at 10 GHz are shown in Figs. 24 and 25.

While the results do vary slightly for the two channels (as they have done in other cases of orthogonal channels), basically we observed 18 dB of gain at 10 GHz and an on-off ratio of more than 25 dB. This gain figure is equivalent to the best that has been reported in the literature for a dual-gate FET structure at 10 GHz. The off gain is not the device's true value. At a control gate voltage of -1 V, the power output is approaching the sensitivity of the measuring system. With the device fully pinched-off ($V_{g2} \lessapprox -2$ V) the linear gain (loss) cannot be accurately measured but is probably in excess of -20 dB. Thus the true on-off ratio at 10 GHz seems to be more than 35 dB, which agrees with measurements made with the network analyzer on other devices (see Fig. 19).

The conclusions from these data are very encouraging. The basic dual-gate structure seems to have enough gain to provide the broadband operation we are seeking, while its on-off isolation capabilities are also sufficient for the switching operations for which it is intended.

These results ended this year's measurement efforts on an optimistic note. All of the data taken thus far indicated the feasibility of producing the kind of broadband lossless multiport switches being sought. Additionally, the coplanar test fixture, which was nearing its initial use, held the promise of finally being able to fully characterize the devices — a very important and major step toward designing the demonstration circuits proposed for the contract.

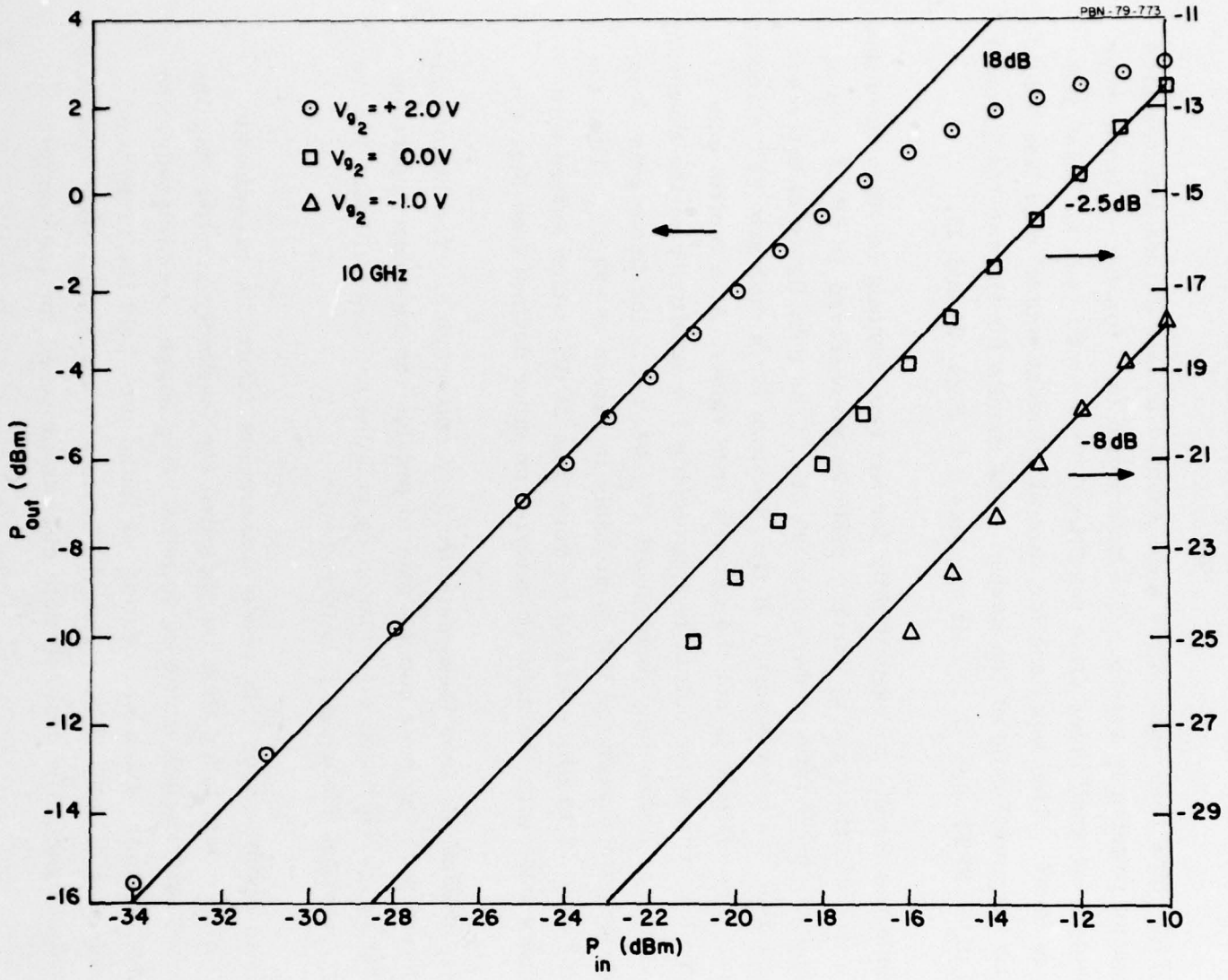


Figure 24. Gain vs. Input Drive, SPST Device Right Side Channel.

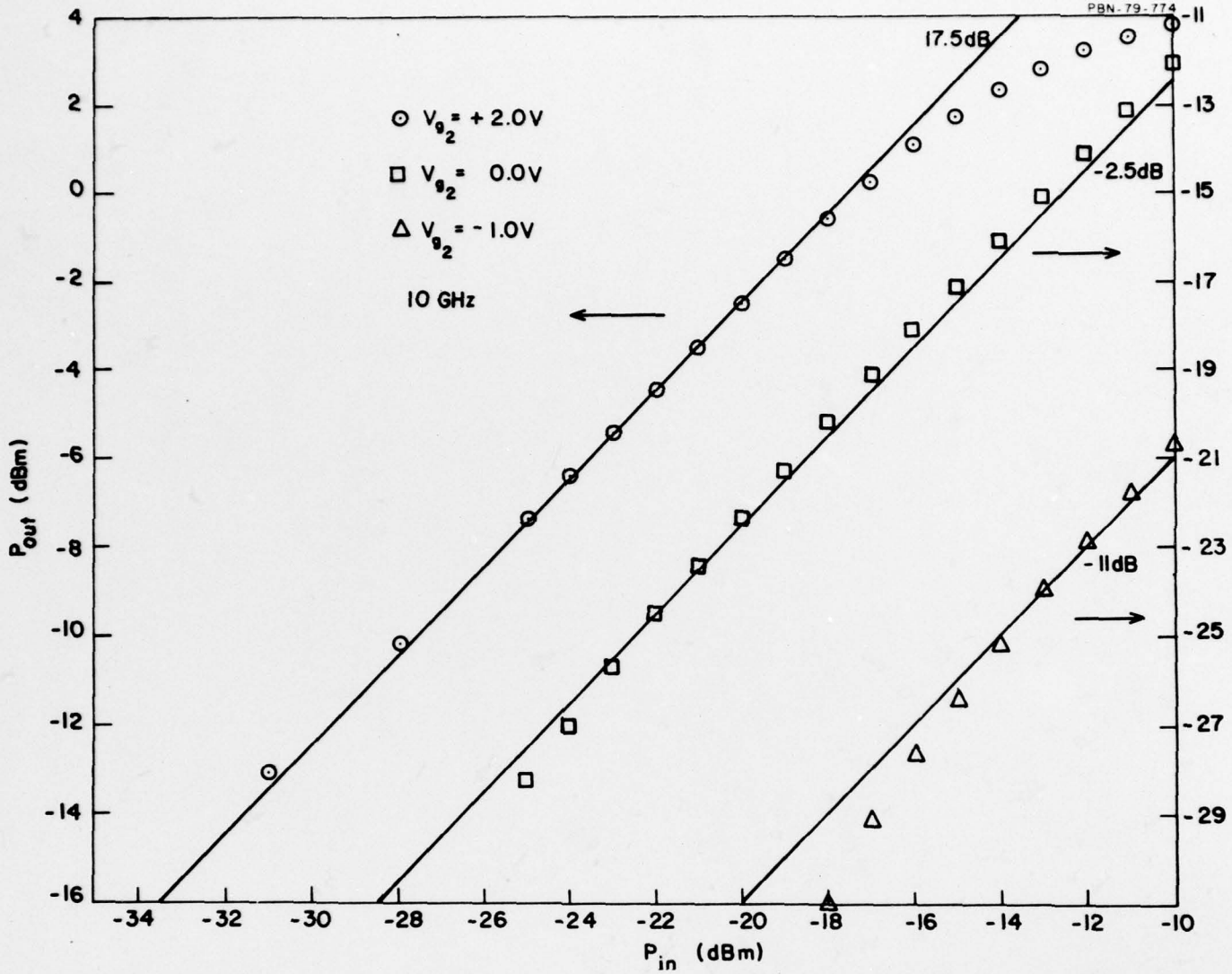


Figure 25. Gain vs. Input Drive, SPST Device Bottom Channel.

5.0 SUMMARY

In the past year, we have designed and fabricated two different dual-gate FET structures which functionally operate as multipole, multithrow switches with gain. We have achieved gains of 18 dB at 10 GHz from a more conventional dual-gate structure. This result is comparable to the best reported in the literature. We have also measured on-off ratios in excess of 30 dB and channel-to-channel isolation in excess of 25 dB in a multiport structure.

Because of the many difficulties in handling multiport structures such as these, we have not yet been able to demonstrate actual microwave signal switching. However, near the end of this report period we developed a new measurement technique which has the potential of eliminating many of the existing difficulties.

6.0 PLANS FOR THE FUTURE

1. Develop the technology necessary for devices operating at Ku-band frequencies.

2. Continue developing automated dc characterization techniques for evaluating devices on-wafer.

3. Develop and exploit the coplanar waveguide structure as a technique for characterizing the switch devices at microwave frequencies.

4. Develop a model of the dual-gate switch structure capable of predicting gain and phase performance over at least an octave bandwidth.

5. Design and fabricate a 7 to 17 GHz bandwidth single-pole, four-throw lossless switching circuit.

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